A quick guide to microfabrication

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Process integration

Explain the process flow step-by-step:

List of main steps:
-deposition material X
-lithography, pattern Z
-etching material X (+ strip)
-diffusion B/P
-implantation B/P
-epitaxy (Si on Si)
-bond wafer X to wafer Y
-CMP of material X
-annealing @ X^{o}C, Y min

Photoresist spinning is required as a separate step only if it is not related to lithography step (e.g. backside protection).

Remember your lab technician: she reads the instructions line by line, and performs one step at a time.

Lithography

Lithography consists of water removal bake, HMDS priming, resist spinning, bake, alignment, exposure, development, bake, microscope check. Now it is said.

From now on, when you say “lithography”, all those steps are assumed automatically.

There is no such thing as “lithography on both sides”. You have to tell which side is processed first; and make a separate step for processing the other side.

When there is a patterned film or structures in silicon, there must have been a lithography step !

Step-by-step

A list of process steps in strict chronological order.

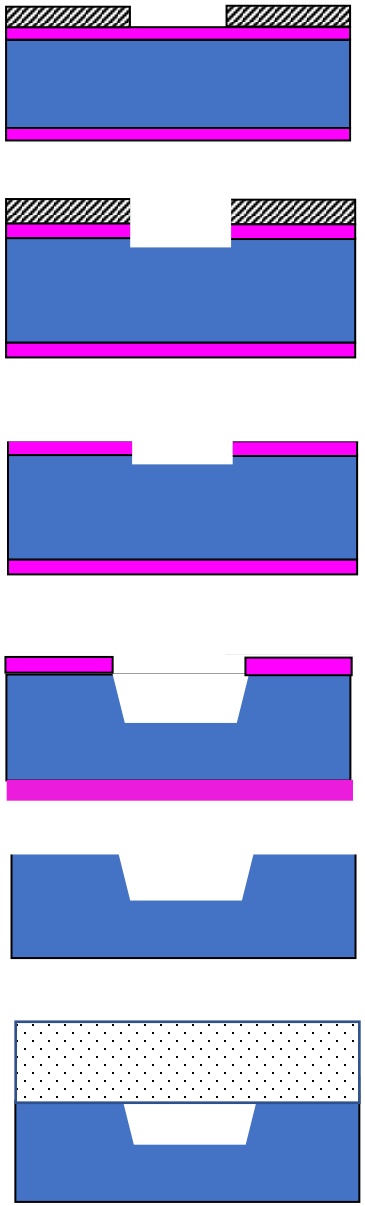
0. Wafer selection: (100) silicon, 380 µm thick
1. Thermal oxidation (both sides simultaneously)
2. Lithography on front side
3. Oxide etch in RIE + strip resist (oxide remains on back)
4. Silicon etch in KOH, oxide hard mask
5. Remove all oxide in HF
6. Anodically bond glass wafer on top

Always tell which material you are processing,
e.g. etch oxide; evaporate gold; and not just etch or deposit.

If you can, provide details: oxide thickness 1 µm,
tungsten deposition by sputtering; Al RIE in Cl_2;
LPCVD nitride @800^{o}C.

Do not invent details ! Check facts from literature,
or leave details out. Mistakes reduce points !

Details aside, you can also explain requirements:
Etch nitride selectively against oxide;
Anneal implant damage and recover crystallinity;
Deposit tungsten with good step coverage.



Wafers

Wafer standard thicknesses 380 µm, 525 µm, 625 µm.

Use 500 µm as a default option.

Use SSP as default.

Use DSP if you do litho on both sides (remember: one side litho first, then etch. Then another litho and etch).

SOI and epi are normally double side polished.

Epi or SOI requires special reasons (very expensive).

Thickness and linewidth

MEMS linewidths are 1-10 μm.

Thin films are ~ 1 μm thick in microdevices.

CMOS linewidths are 10-100 nm.

CMOS film thicknesses are similar to linewidths

Thin film thickness in nanodevices ~ same as their linewidth (aspect ratio ~ 1:1).

Cross sections are (practically) never drawn to scale.

Oxides

SiO_2 is obtained by thermal oxidation @1000^oC

Thermal oxides (incl. BOX) are grown. 1 µm is thick.

Note: Thermal nitridation does not exist (in microfabrication)

Oxide is generic term for both thermal and CVD oxides.

CVD oxides are deposited (as D in CVD hints)

@400^oC by thermal CVD

@300^oC by PECVD

@RT by spontaneous reaction = native oxide ~1-2 nm

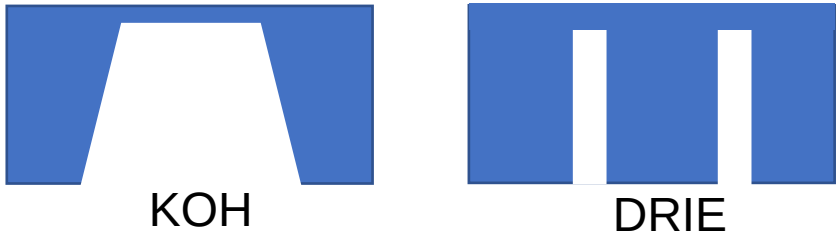
@RT by oxygen plasma or nitric acid, ~1-2 nm

Thin film deposition

<Si>	CVD epitaxy @1000^{o}C (can be thick, up to 100 μm)
poly-Si	LPCVD @600^{o}C
a-Si	PECVD @ 300^{o}C
Si_3N_4	LPCVD @800^{o}C
SiN_x	PECVD @300^{o}C
W	CVD @400^{o}C, also sputtering
all metals	sputtering, evaporation @RT
Cu, Au, Ni	electroplating @RT (can be very thick, 10's μm)
Al_2O_3, HfO_2	ALD @200-300^{o}C (ALD films are thin, <100 nm)

assume 1 μm unless you have reasons to argue otherwise

Etching (1)



Silicon is etched either:

- DRIE with resist or oxide mask (never nitride)
- KOH with oxide or nitride mask (never resist)

Silicon DRIE is the only DRIE there is (on this course).

Oxide is etched either:

- HF with resist mask, isotropic (selectivity ox:Si ~ ∞, ox:nit ~100:1)
- RIE in CHF_3 with resist mask (selectivity ox:Si ~ 10:1, ox:nit ~ 3:1)

Nitride is always etched in RIE (SF_6, CF_4, CHF_3), both to make patterns, or blanket removal.

Note: nitride and silicon are both etched by SF_6, CF_4.

Etching metals

Al	wet with H_3PO_4	} small linewidths by RIE
	RIE with Cl_2	
W, Mo, Ti	wet by H_2O_2	
	RIE by F* (SF_6) etches also nitride and silicon	
Cr, Ni, Cu	wet by acids (Cu does not have RIE !!)	
Au, Pt	wet by aqua regia	

Ion beam etching works for all (if they are very thin, since very slow)

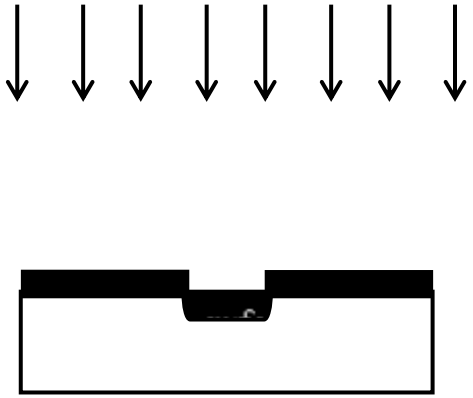
Other metallization options (if deposit+litho+etch does not work):

Lift-off (litho + deposit + resist strip) for hard-to-etch materials & multilayers

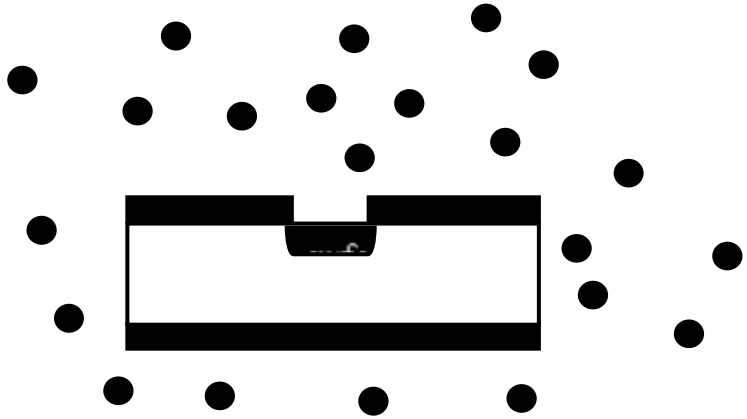
Damascene for copper (oxide etching + Cu plating + Cu CMP)

Lithography + plating is an option for Cu, Ni, Au

1- or 2-sided processing ?



Beam processes 1-sided



Immersion processes 2-sided

-photon beams (=lithography)

-atom beams (=evaporation)

-ion beams (=implantation)

-mixture of beams (=plasmas)

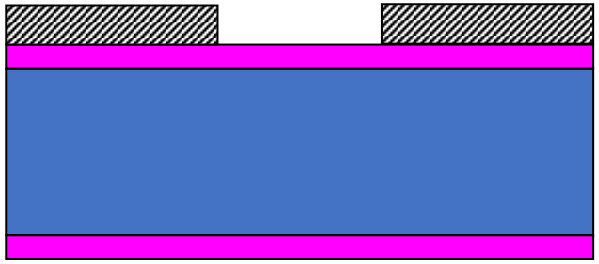
-liquids (=wet etching)

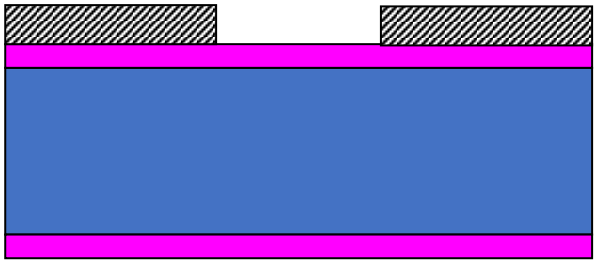
-liquids (=cleaning)

-gases (= oxidation, diffusion)

-gases (=CVD)

Mind the backside !





Oxide wet etch in HF

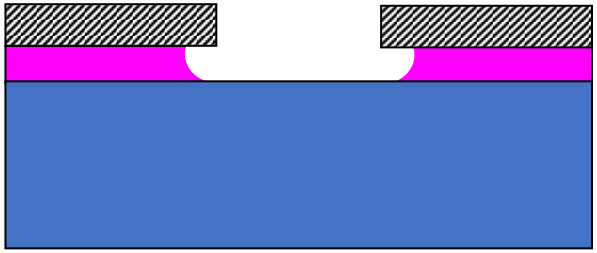
Undercut, isotropic

High selectivity

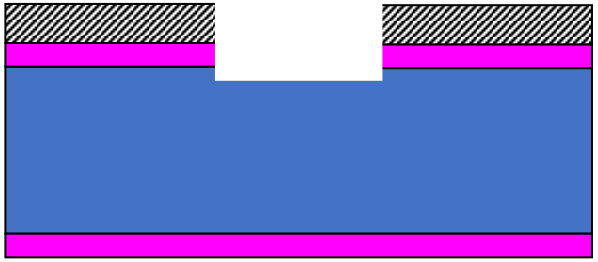
Oxide plasma etch in CHF_3

Vertical walls, no undercut

Not so good selectivity

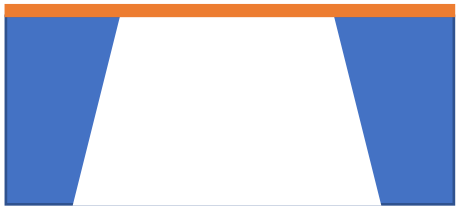


Film removed from backside



Film remains on backside

Membranes and holes



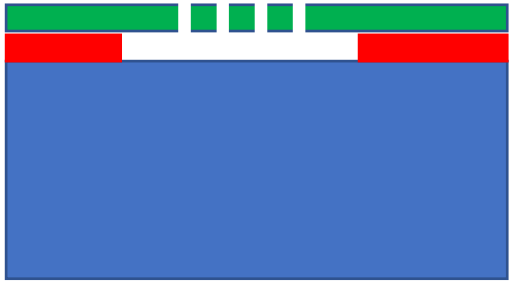
Nitride membrane is usually last step. Not first because it is not strong enough to tolerate processing (spinning, high temperatures…).

Oxide membrane cannot be done because of compressive stresses.

Solutions: etch silicon as the last step. Or leave some supporting silicon. SOI device Si also good mechanical support.

Wafers with thru-holes cannot be further processed because resist can not be spin coated anymore (because vacuum chuck does not work, and because resist would flow into deep the holes).

Solutions: etch thru-holes last. Or make peeling mask, and you do not have to do litho after holes.



Once you have made something free-standing, you cannot do lithography anymore, because resist would fill the cavity. Besides, the thin released structure is very fragile.

Solution: do the release etch last.

Avoid stupid mistakes

When the question is about step-by-step process flow do not tell about HMDS priming, spin coating, bake, alignment, exposure…

When the question is “Lithography”, and it is 6 points worth, then you should spend approximately 30-40 min answering it. It must be pretty substantial, and one paragraph certainly won’t do.

Do not grow 10 µm thick thermal oxides.

Do not grow epitaxy on oxide.

Almost always there is a litho step before etch step (exceptions: spacer formation; removal of oxide diffusion mask, …)

Comparing A and B means finding similarities and differences between the two. Listing everything you know about A and everything you know about B will not bring you many points.

Standard modules

Patterning a thin film:
-deposition
-lithography
-etching + resist strip

Diffusion:
-thermal oxidation
-lithography
-oxide etching + resist strip
-wafer cleaning
-thermal diffusion
-oxide removal in HF

Thru-silicon by KOH from back:
-SiO_2 thermal
-resist spin on front (protection)
-lithography on back
-HF etch SiO_2 + strip
-etch <Si> in KOH

DRIE with hard mask:
-oxide deposition
-lithography
-oxide etch + resist strip
-DRIE of <Si>

Ion implantation:
-lithography
-ion implantation
-resist strip
-wafer cleaning
-annealing

Surface MEMS:
-deposit sacrificial layer
-lithography
-etch sacrificial layer + strip
-deposit structural layer
-lithography
-etch structural layer + strip
-isotropically etch sacrificial layer and release structural layer

Damascene:
-oxide CVD
-lithography
-oxide etching + resist strip
-copper electroplating
-copper CMP