Aalto University
School of Electrical
Engineering

Configuring Chip'n Dale tape-out flow

Marko Kosunen

Department of Electronics and Nanoengineering
Aalto University, School of Electrical Engineering
marko.kosunen@aalto.fi

February 24, 2024

Outline

Course objective and introduction

Course objective and introduction

Flow-construction course - preparations to Tape-out course

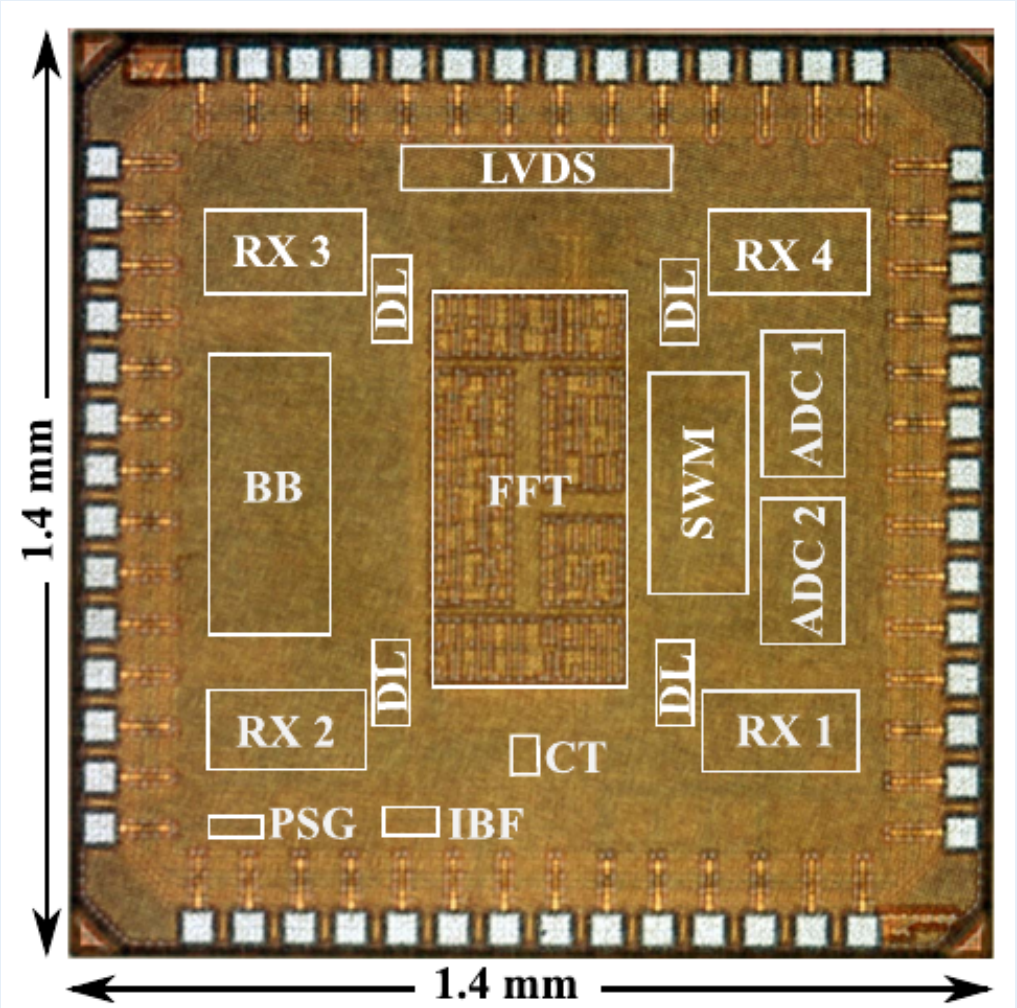
- Motivation
  - Programmatic design flows are becoming increasingly popular (ChipnDale. ChipYard, plus various unknown flows developed in various universities.
  - Chip construction flows make it possible to teach Tape-out already at the Bachelors-stage. (UC Berkeley profs. received an award about this in ISSCC2024)
  - In general, setting up the design environments is just one area of microelectronics desing. It is NOT the job of generic sysadmins. They can not do it.
- Objectives
  - Teach you how to configure a Chip'nDale design environment for a semiconductor process.
  - Construct a complete flow for *student* flow that can be used for Tape-out course.
  - Improve documentation of Chip'nDale project.

Tape-out Course objective

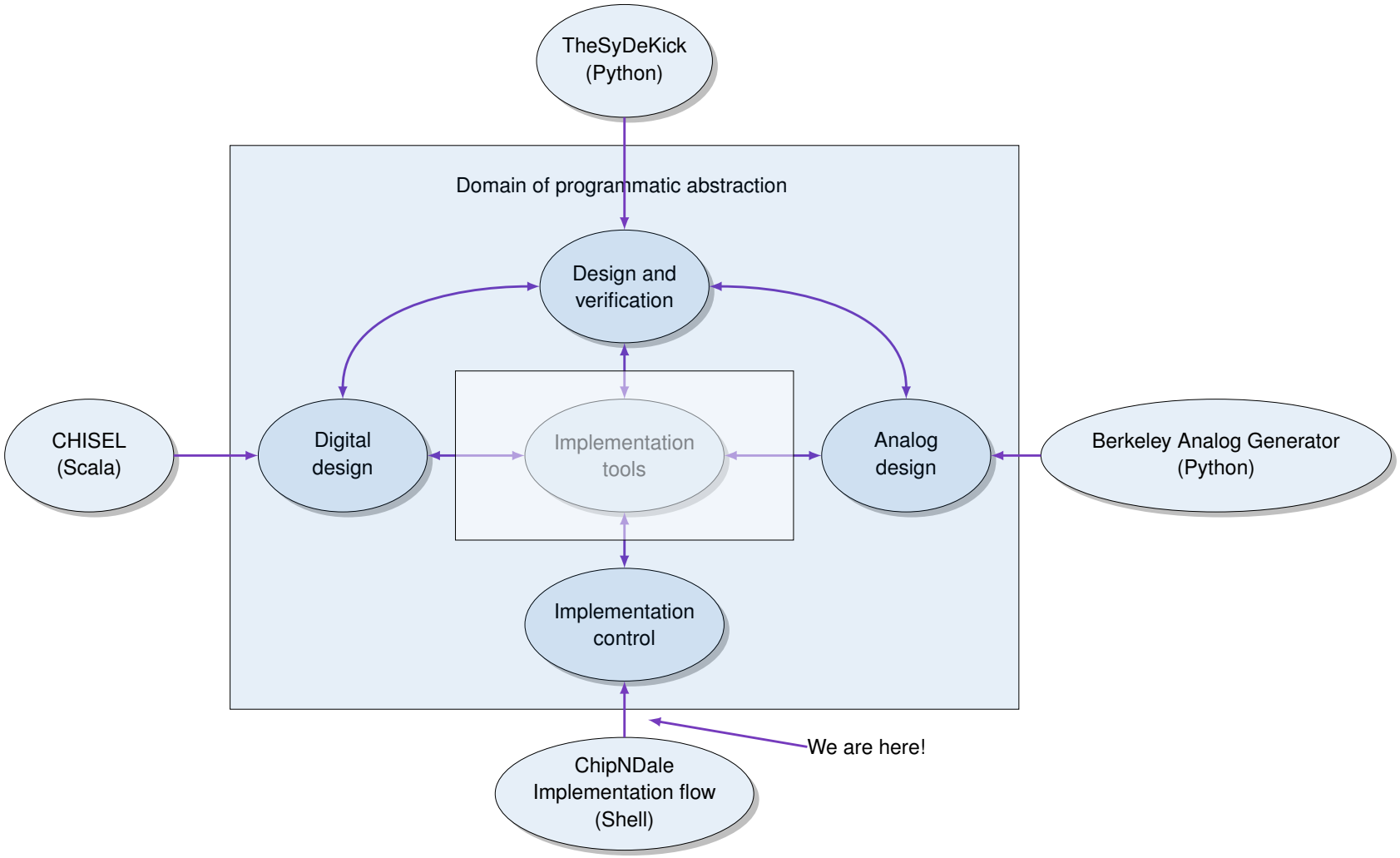
- Familiarize the student to *one* variant of Tape-out ready chip construction flow
- This is achieved with the following tasks
  - Familiarising oneself to a *template-flow*: providing a LVS clean, DRC checked Chip GDSII with IO's in place.
  - Cloning the template to a project, and configurring the project with project-dependent parameters.
  - Design of custom analog and digital blocks and modifying the IO's and floorplan accordingly
  - Creating a chip toplevel in Virtuoso.
  - Running the flow for the toplevel.

System on Chip

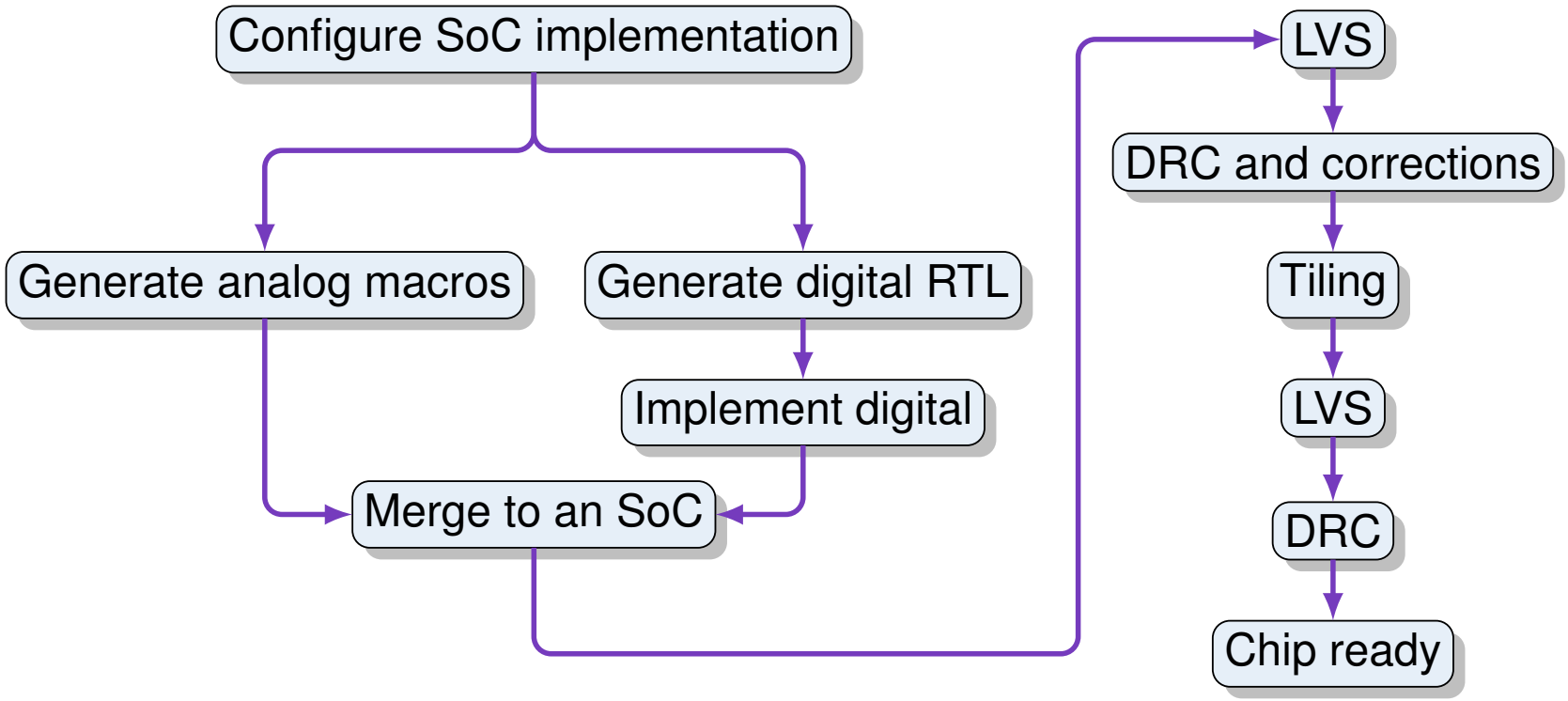
Receiver with FFT spectrum estimation



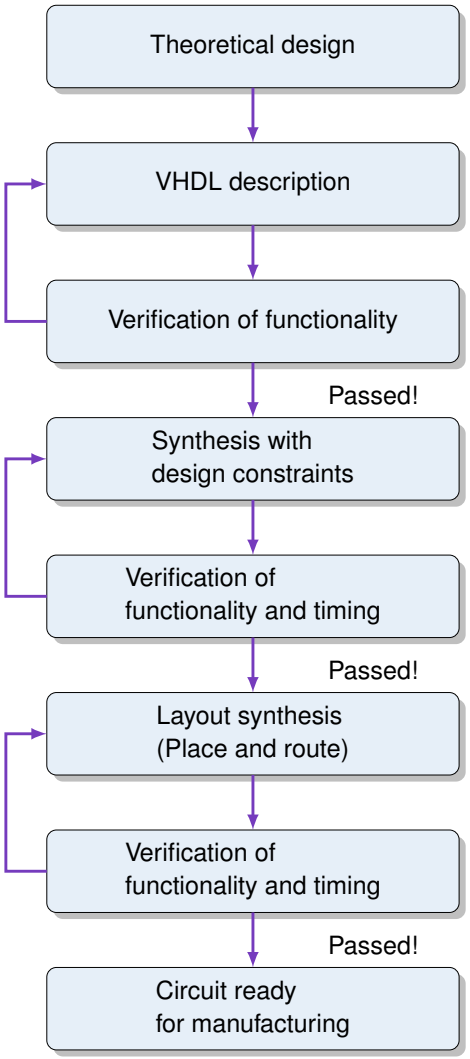
Big picture


TheSyDeKick
(Python)
Domain of programmatic abstraction
Design and
verification
CHISEL
(Scala)
Digital
design
Implementation
tools
Analog
design
Berkeley Analog Generator
(Python)
Implementation
control
We are here!
ChipNDale
Implementation flow
(Shell)

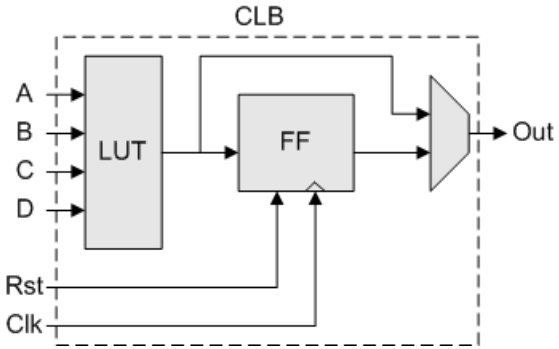
SoC implementation environment



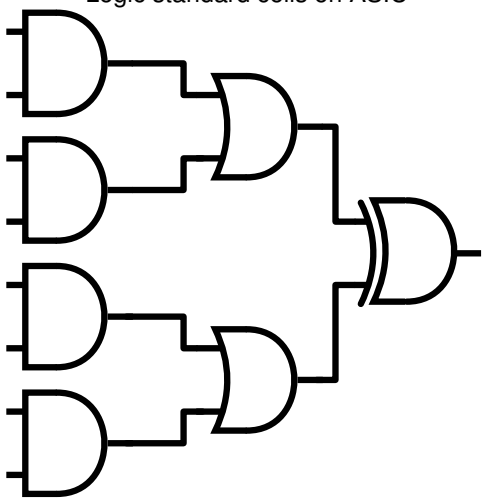
Digital implementation flow



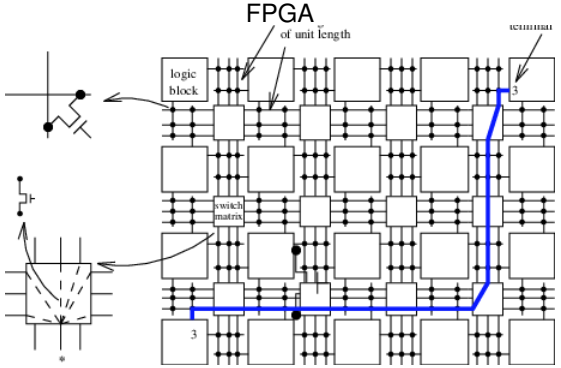
Logic elements on FPGA



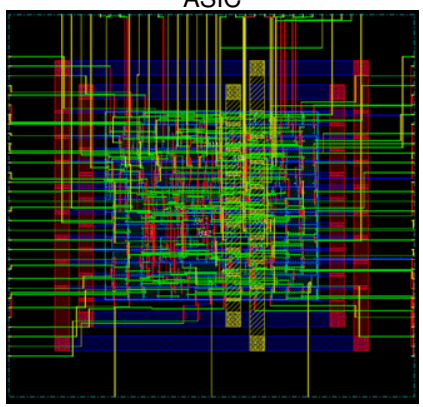
Logic standard cells on ASIC



FPGA



ASIC



Current status

- We have a Flow template published at *https://gitlab.com/chipndale*
- It is poorly documented and does not have *any* process configuration in place.
- In our lab, we are using several similar flows having the working process setup.
- Objectives:
  - Fully configure the flow for gpdk045 OR tsmcN16 education version (i'd pick tsmcN16).
  - Cadence GPDK045 has digital flow in place, but the support is limited for Cadence tools only, and the analog part is missing a lot of configurations.
  - tsmcN16 has it's *production* flow in place, but the *student* flow has nothing. However, setting up the flow based on the production version should be straightforward.
  - Neither of the processes have padring templates ready.
  - We have some flow documentation slides in the lab, but those should be cleaned up from process references.

Course completion

- Assumption is that you are able to run the flow already. That will (preferably) not be taught on this course.
- I have created 21 issues that must be completed to set up a process flow. (for gpdk045, part of these have been closed already)
- At the end, we should have at least one working student flow, and improved documentation at ChipNDale about how to do that.
- I know how to do it, so we will have exercise sessions where I can guide you through the process.
- At the end of the course, you will (individually) present what you did, and demonstrate the working flow(s) and improvements made to documentation.
- 5 credits admitted.

Expectations

- I will work with you, ask me if you get stuck.
- This course is very much learning by doing.
- Every semiconductor process is configured similarly, and these are just tasks to be completed, you'll learn while doing them.
- I hope that you get some reward of eventually working flow, and thinking that this enables world class education in our university AND dissemination of the Chip'nDale flow. Flows are emerging, not omnipresent, and we are at the forefront.