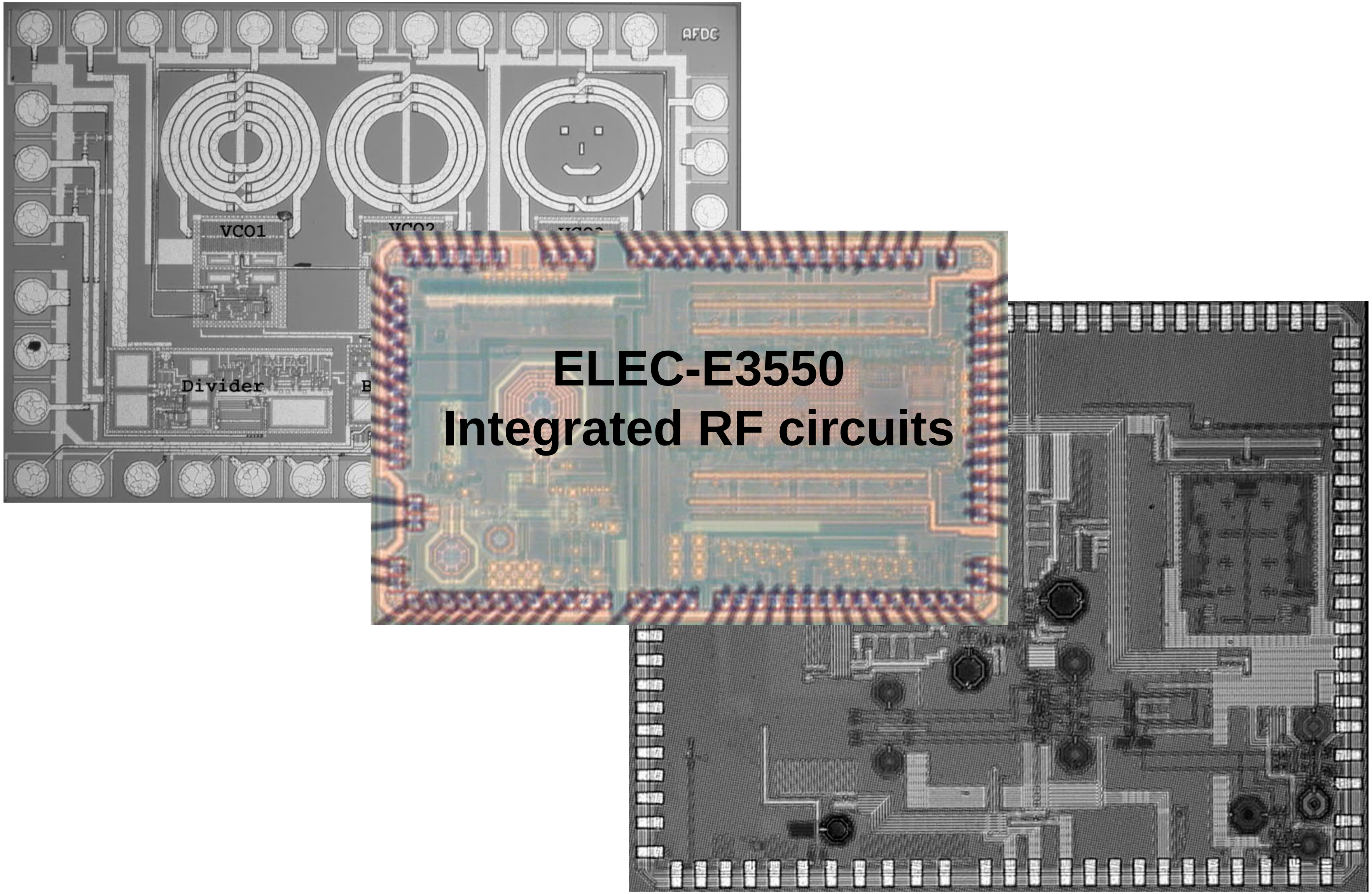



# ELEC-E3550
# Integrated RF circuits

Aalto University
School of Electrical
Engineering

**Department of Electronics and Nanoengineering**
Kari Stadius, Mahwish Zahra, Kalle Spoof

**Integrated RF circuits**
**Spring 2019**

# Topics of the previous lecture

**Concepts related to mixers**

"*mixing*" = multiplication in time-domain = frequency shift in frequency domain

Conversion gain, SSB / DSB NF, IIP2 / IIP3, ICP, isolation

**Active mixers**

Cascode amplifier

Active mixer

Single-balanced mixer

Double-balanced mixer

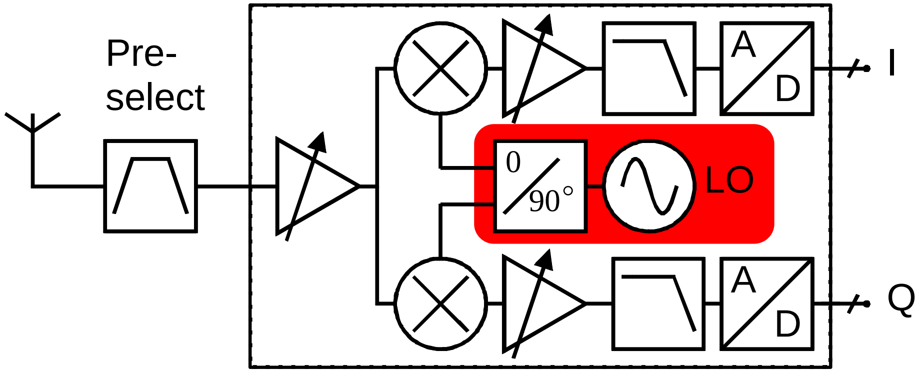
**Gilbert cell mixer**

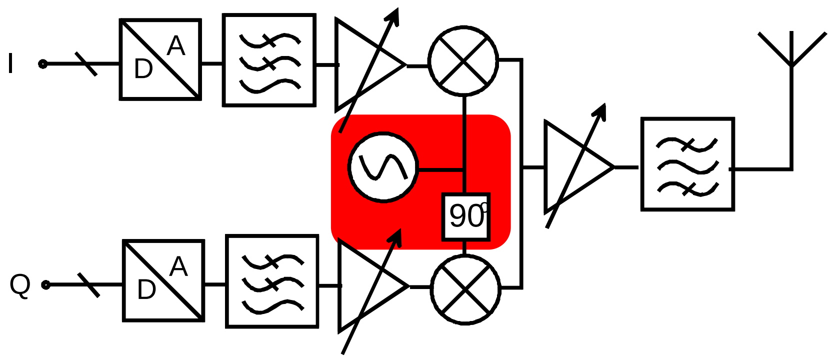
**Passive mixers**

Voltage-mode passive mixer

**Current-mode passive mixer**

# Frequency Synthesizers (SX)




- System level & concepts
- SX principles

- Phase-locked loop
  - ”theory” / CP-PLL / ADPLL

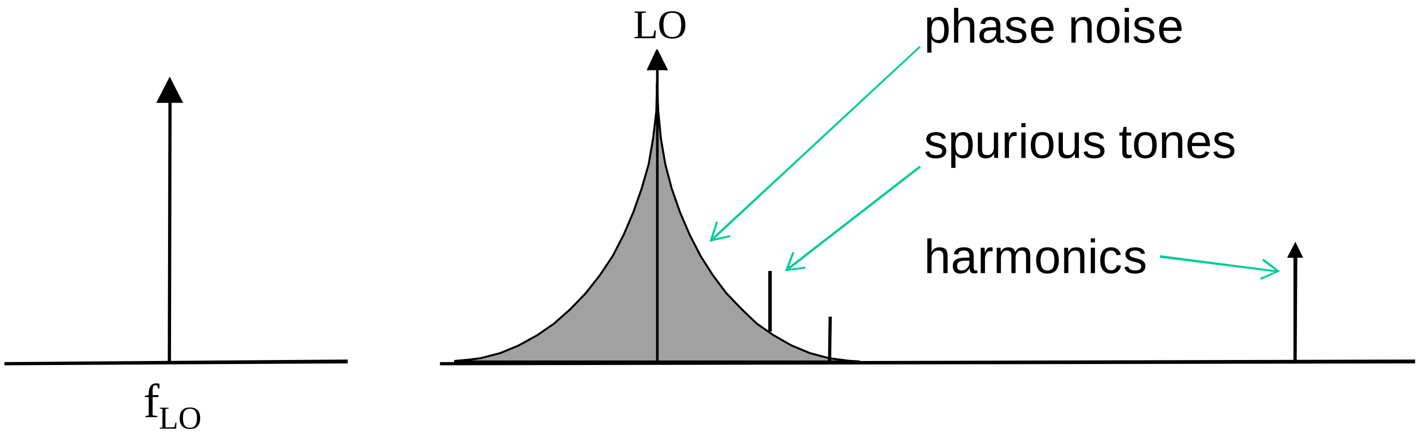
*Break*

- Oscillators
  - Ring & LC
- Frequency dividers
- Quadrature generation

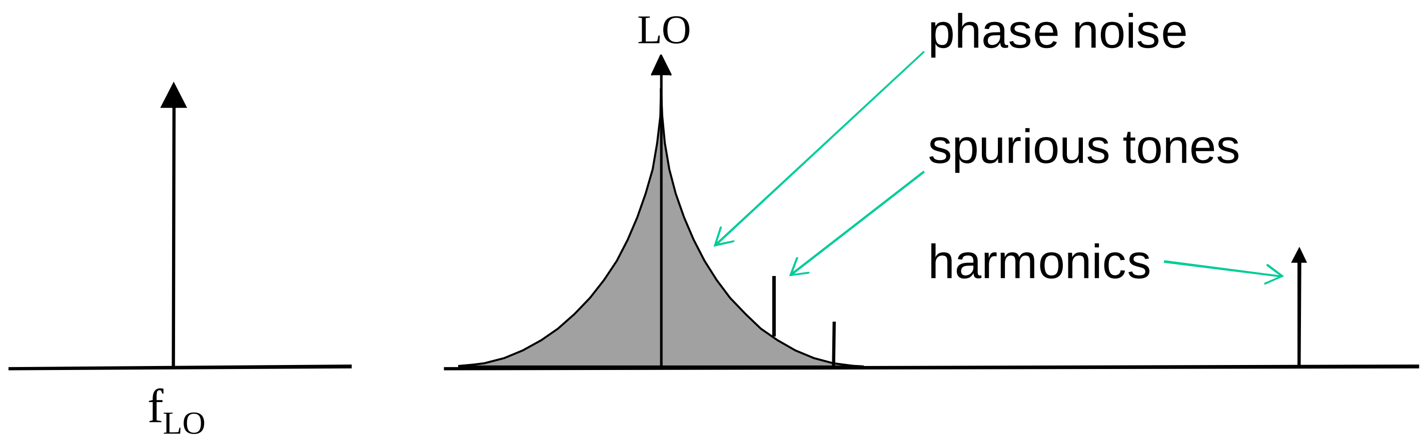
***Break***

Exercises & Homework

# SX Requirements



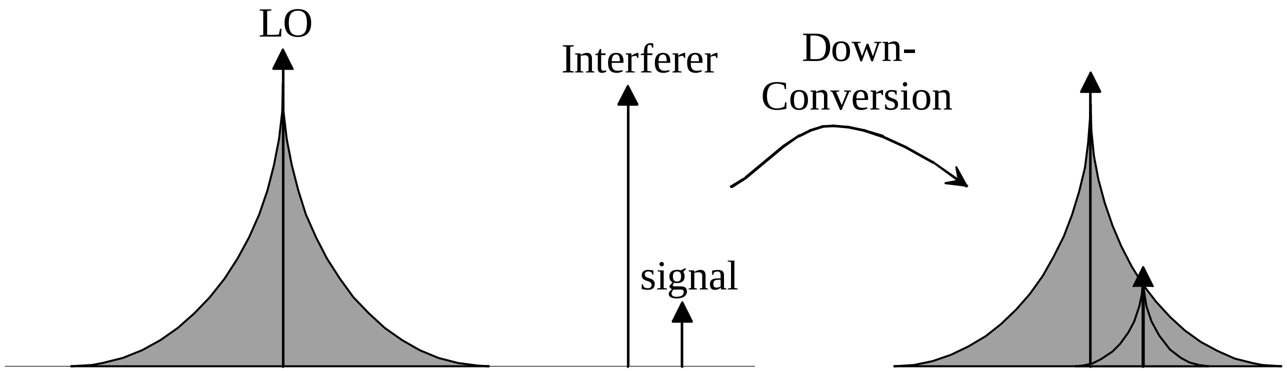
# SX Requirements



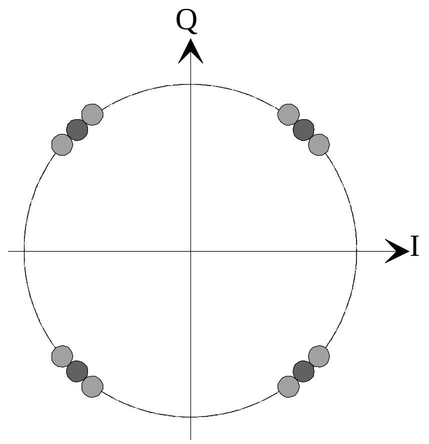

- Frequency span --- cover the required bandwidth + margin for PVT
- Channel spacing & settling time
- Phase noise
- IQ-generation --- Amplitude and phase imbalance (IRR)

# Impact of Phase Noise

Reciprocal mixing



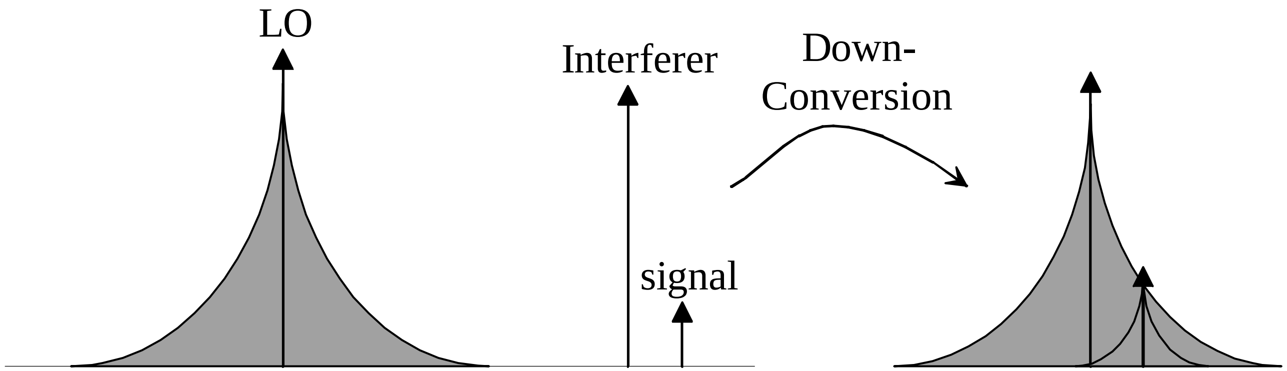

Phase noise impacts IQ-constellation



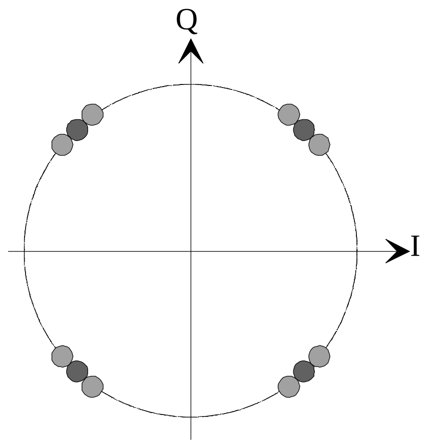

In TX, phase noise causes out-of-band spurious emission.

# Impact of Phase Noise

Reciprocal mixing




Phase noise impacts IQ-constellation




In TX, phase noise causes out-of-band spurious emission.

Phase noise requirement depends on:

- Channel spacing
- Modulation method (eg. compare QAM-16 vs. QAM-256)
- Required sensitivity and selectivity
- Specified environment (”hostile” / ”friendly”)
- TX: emission mask

# Phase Noise Specifications

Phase noise specification for SX given either by

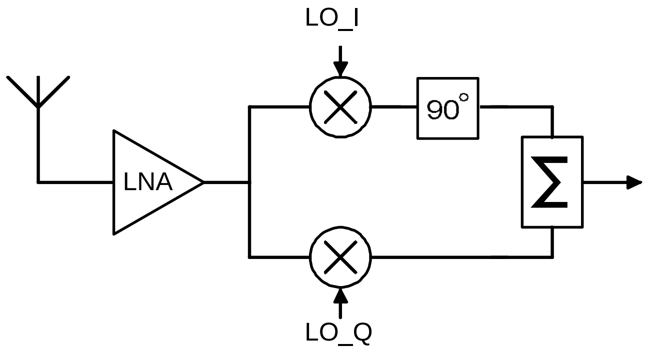
- N/C at certain offset, e.g  N/C@1 MHz < -120 dBc/Hz
- Integrated N/C profile → can be then converted to jitter spec

| System | Band [MHz] | Ch. spacing [kHz] | N/C [dBc/Hz]@kHz | norm-N/C* [dBc/Hz] |
|---|---|---|---|---|
| IS54 | 824-849 | 30 | -115@60 | -132 |
| GSM | 880-915 | 200 | -141@3000 | -125 |
| DECT | 1880-1900 | 1728 | -97@1800 | -91 |
| WCDMA | 1920-1980 | 5000 | -129@8000 | -111 |
| WLAN (b) | 2400-2483.5 | 22000 | -103@1000 | -105 |
| BlueTooth | 2400-2483.5 | 1000 | -109@1000 | -111 |
| GPS | 1575.42 | - | -95@1000 | -93 |
| DOCSIS** | 47-862 | 6000 | -82@10 | -100 |
| DVB-S | 10700-12750 | fixed LO1 | -95@100 | -131 |

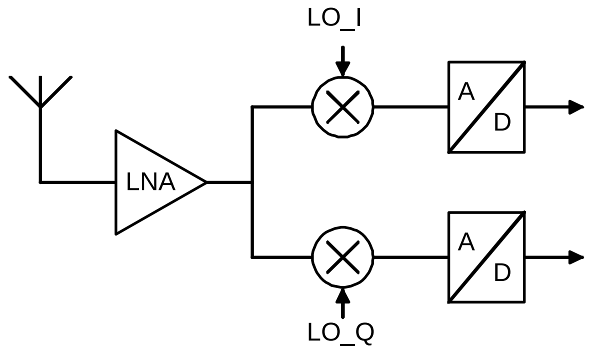
* Normalized to 2GHz and 1MHz, N/C~$(fo/fm)^2$        **data over cable-TV

# IQ Imbalance

Hartley Receiver




DCR




- LO signals (I) and (Q): equal amplitude (A) and 90-degree phase shift ($\phi$)
- $\Delta A$ and $\Delta\phi$ results in imperfect image rejection or reduced SNR for DRC
- Every signal path element contribute to IRR, but usually LO imperfections dominate
- Image-Reject Ratio (IRR) is a measure of LO signal imbalance

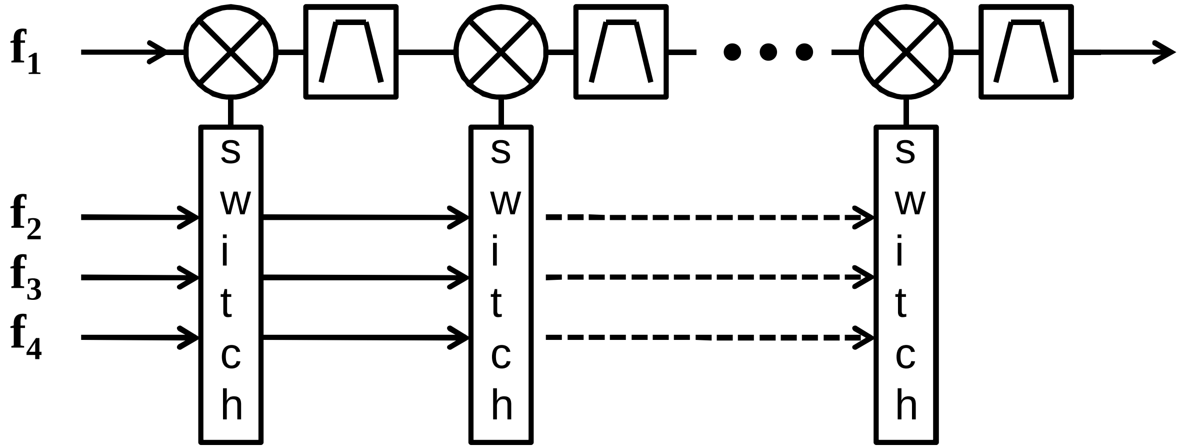
$$IRR = \frac{1 + 2A_{bal}\cos\Delta\theta + A_{bal}^2}{1 - 2A_{bal}\cos\Delta\theta + A_{bal}^2}$$

- Typically DCRs need **IRR > 30 dB** → $A_{bal}$ < 0.5 dB and $\Delta\theta$ < 4°
- LO chain often includes limiting amplifiers → phase error remains a challenge

# Frequency Synthesis Methods

1. Direct analog synthesis — *"DAS"*
2. Direct digital synthesis — *"DDS"*
3. Indirect digital synthesis — *"PLL"*
4. Indirect analog synthesis — *"PLL"*

# Direct Analog Synthesis (DAS)




- Filters are filter banks and/or tunable filters
- Amplifiers not drawn
- Chain may include dividers as well

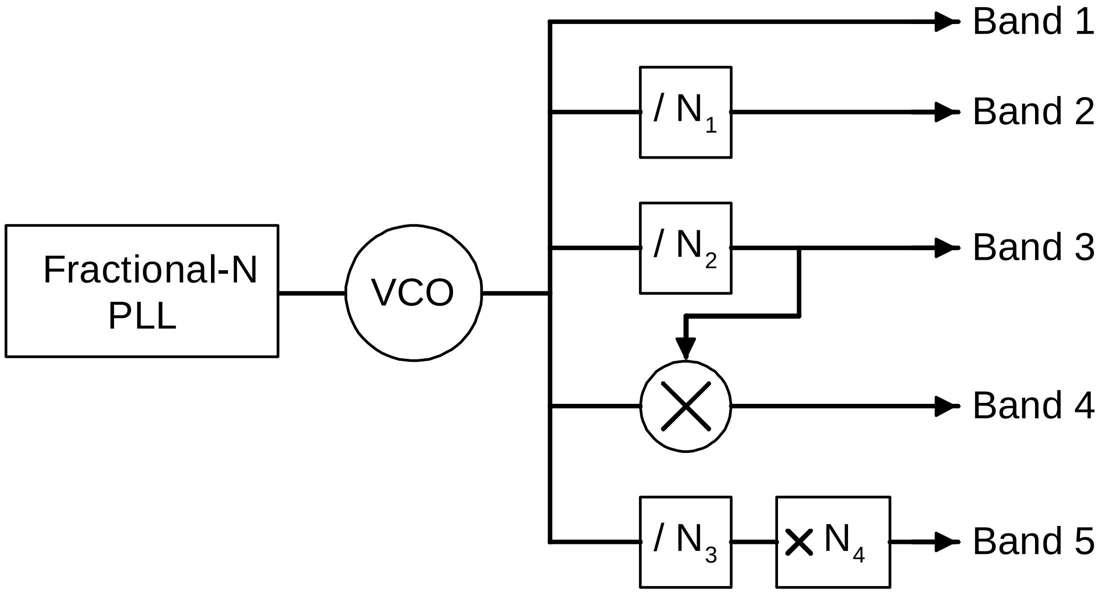
Main problem for RF IC implementation: good filters can not be integrated.

DAS is in use e.g. in measurement instruments – High perf, high price

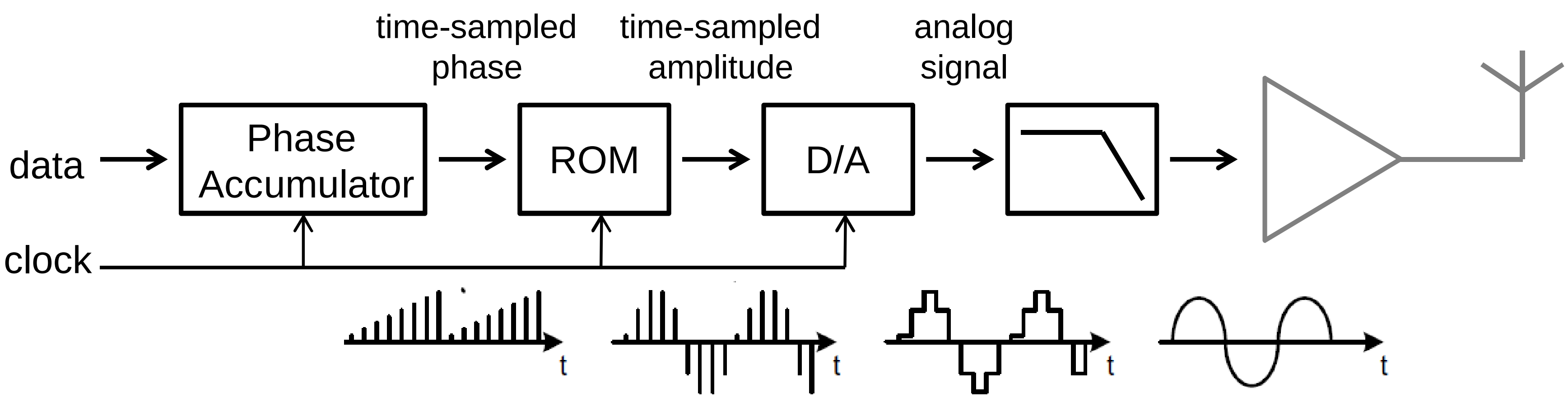
# Direct Analog Synthesis

At RF IC context we may use simplified versions of DAS.

”Manipulate a frequency tone with basic mathematical operators”
- addition → mixer
- substraction → mixer
- division → frequency divider
- multiplication → frequency doubler / tripler



# Direct Digital Synthesis (DDS)




Problems:

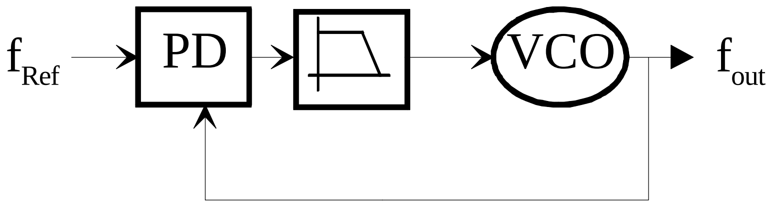
needs a high-speed D/A

needs $f_{clock} > 3^* f_{out}$

DDS is used in base stations and LF radios (e.g. military)

Enables very complex modulations (military)

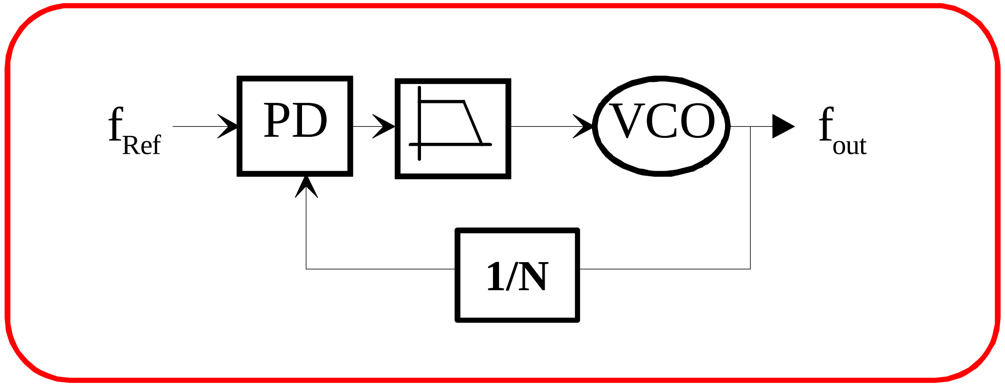
# Indirect FS -- Phase-Locked Loop




Basic idea is to lock the oscillator into the incoming signal using a feedback loop.

Compare to: feedback amplifier analysis in electronics

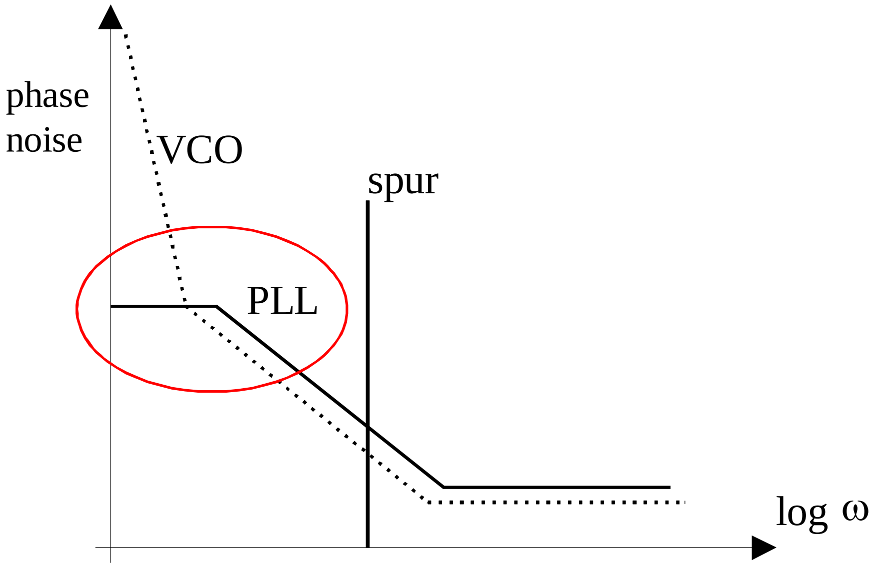
feedback systems in control theory and automation



# Some Books on PLL's

- Many basic text books on RF/analog IC electronics include a chapter on PLLs
  - Razavi: RF Microelectronics,
  - Lee: The Design of CMOS RF IC,
  - Grebene: Bipolar and MOS Analog IC Desing, etc.
- U. Rohde: many books on PLL's, not RF IC oriented
- F. Gardner: Phaselock Techniques
- R. Best: Phase-Locked Loops: design, simulation and applications
- J. Crawford: Frequency Synthesizer Design Handbook
- D. Wolaver: Phase-Locked Loop Circuit Design
- C. Vaucher: Architectures for RF Frequency Synthesizers
- D. Banerjee: PLL Performance, Simulation and Design (wireless.national.com)
- ... and many more ☺

# Typical Results of Linear Analysis




PLL performs a high-pass filtering for the phase-error → flat in-band noise

# Fractional-N Concept

**Integer-N PLL:**

- reference frequency = channel spacing
- if N is very large
  - stability requires loop-BW < $f_{ref}/10$ → loop-BW small
    → long settling time & poor phase noise reduction at high offset
  - ref. source & PD noise is multiplied by N
- Recall: GSM1800 ch. spacing=200 kHz, N~10000

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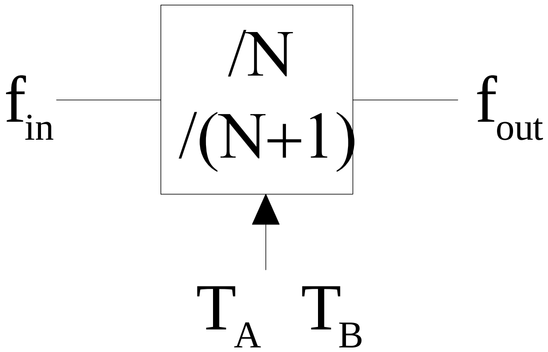
Basic integer-N PLL is not good for small channel-spaced systems
⇒ Improvments on PLL architecture (mixers in loop, dual-loop, frac-N PLL)

**Dual-modulus divider**




$$\frac{T_A}{T_A+T_B}\cdot\frac{f_{in}}{N}+\frac{T_B}{T_A+T_B}\cdot\frac{f_{in}}{N+1}=f_{out}$$

$$\frac{f_{out}}{f_{in}}=\frac{1}{N_{eff}}=\frac{1}{\frac{T_A+T_B}{T_A}\cdot N}+\frac{1}{\frac{T_A+T_B}{T_B}\cdot(N+1)}$$



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# Fractional-N Concept

• With the aid of dual-modulus divider division ratio can be set to N...N+1
Example: $T_A/(T_A+T_B)$=90%, $T_B/(T_A+T_B)$=10% and N=100 => $N_{eff} \approx 100.1$

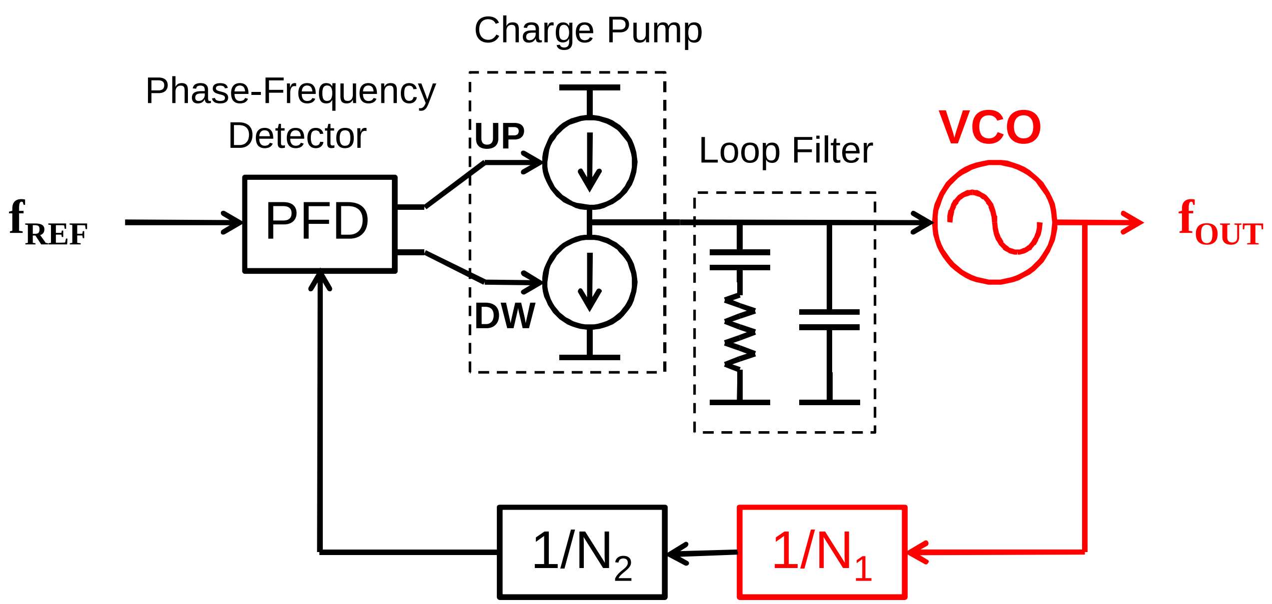
→ Frac-N PLL provides small channel step and still large loop-BW.

• Main problem : ”fractional spurs”
→Can be partly compensated by randomizing the timing
and using ΣΔ noise shaping.

(for details, Razavi presents an easy-to-read presentation in *RF Microelectronics*)

• Frac-N PLL requires more hardware and suffers from high spurios content
and increased noise level compared to int-N PLL.
→ use only when integer-N is not feasible.

# Charge-Pump PLL



# Impact of Technology Evolution

Recall our earlier paradigm changes, e.g.

- GaAs MESFET → Si Bipolar → CMOS
- Superheterodyne receiver → DCR
- Monolithic capacitors:  vertical field → lateral field
- Gilbert cell mixer → current-mode passive mixer

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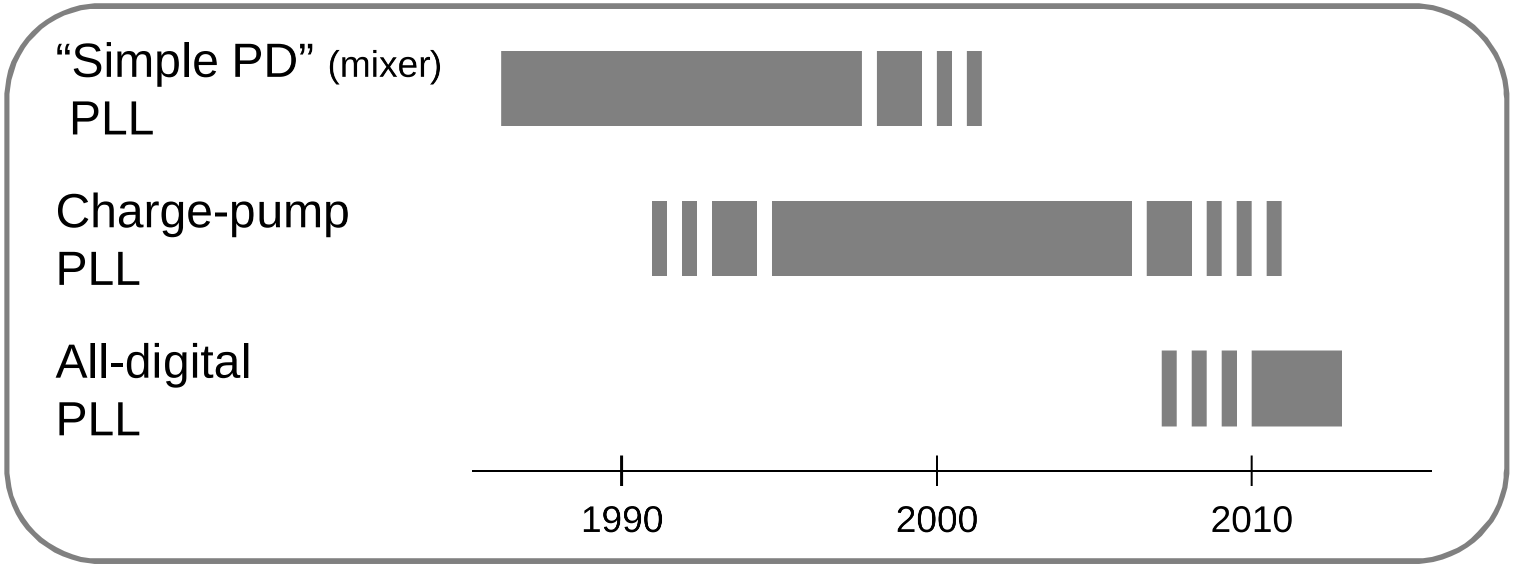
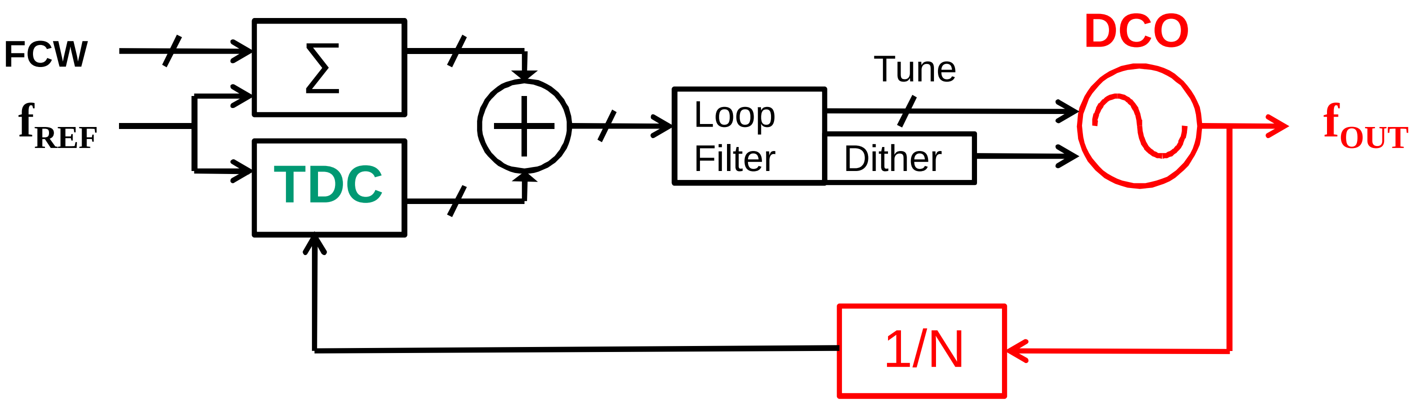



*"In a highly-scaled CMOS technology, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals"*

R. Bogdan Staszewski
Manager of
TI's DRP group

# All-Digital PLL




- Frequency control word (FCW) defines the target frequency
- Time-to-Digital converter (TDC) describes the output frequency with a digital word
- Error signal (digital) is filtered in the digital loop filter
- Digital-controlled oscillator (DCO) is tuned accordingly
- Dithering (compare to frac-N principle) is used to achieve fine frequency step
- Prescaler used to lower $f_{out}$ (only if needed!) (65-nm CMOS: TDC $f_{max}$~1.7 GHz)

# Oscillators

Oscillator is an autonomous device which generates a waveform
→ It converts power from DC to ”AC”

Variable frequency oscillator converts a control signal into frequency
→ information is converted from one mode to another

- VCO – voltage-controlled oscillator
- ICO – current-controlled oscillator
- DCO – digitally controlled oscillator

Oscillator waveform can be

- Sinusoidal : low level of higher harmonics
- Square : high level of higher harmonics, ”clock signal”

- ramp or triangular is used at LF control circuits

# Oscillator Classification

<u>oscillation mode</u>

- Stable (no oscillation)
- Harmonic (sinusoidal)
- Relaxation
- Chaotic

⟺ No correlation !!

<u>oscillator structure</u>

- Phase shift (RC)
- $G_m$-C
- Crystal
- Multivibrator

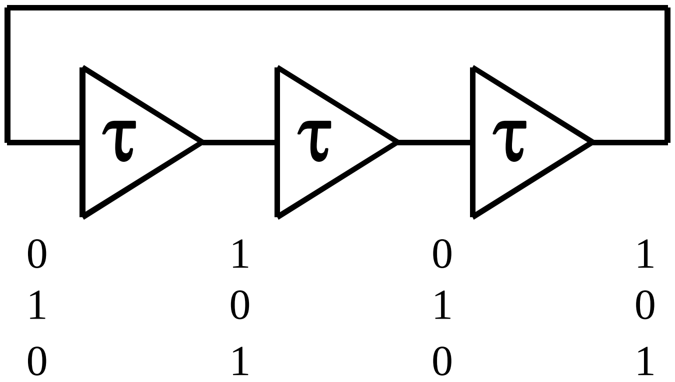
- Ring
- LC

# Oscillator Terms and Figures of Merit

- Tuning Range : ratio of maximum and minimum oscillation frequency
- VCO gain ($K_{VCO}$) and its deviation (linearity)
- Output power (preferably constant)
- supply voltage / current consumption / power efficiency
- Distortion in ”sinusoidal” oscillators
- Temperature stability ($\Delta$freq/$\Delta$T)
- Pushing (PSRR) ($\Delta$freq/$\Delta$supply)
- Pulling (load) : Frequency shift caused by load impedace variation
- Pulling (injection) : Frequency shift caused by external disturbance
- Phase Noise / Jitter
- Die Area (IC implementation) / Component count (discreate circuits)

$$FOM \propto \frac{Tuning\ Range}{Phase\ Noise * Power\ consumption}$$

# Ring Oscillator




$$f_{osc} = \frac{1}{2\tau N}$$

$$\tau \propto \frac{C_{load}}{I} \quad \Rightarrow \quad f_{osc} \propto \frac{I}{C_{load} N}$$

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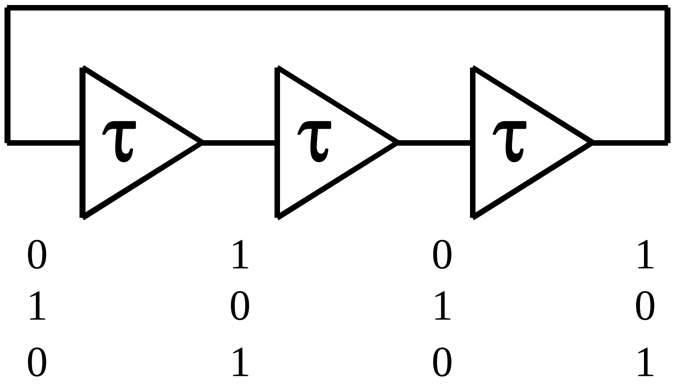
# Ring Oscillator

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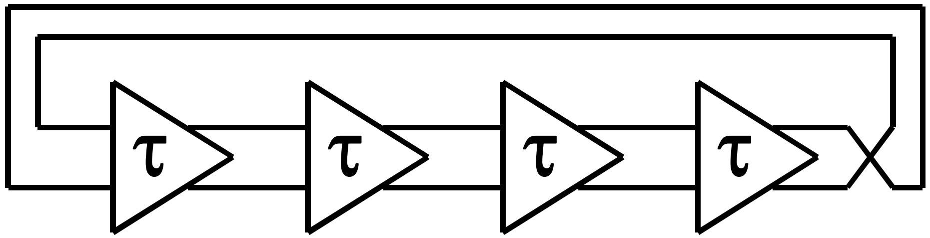
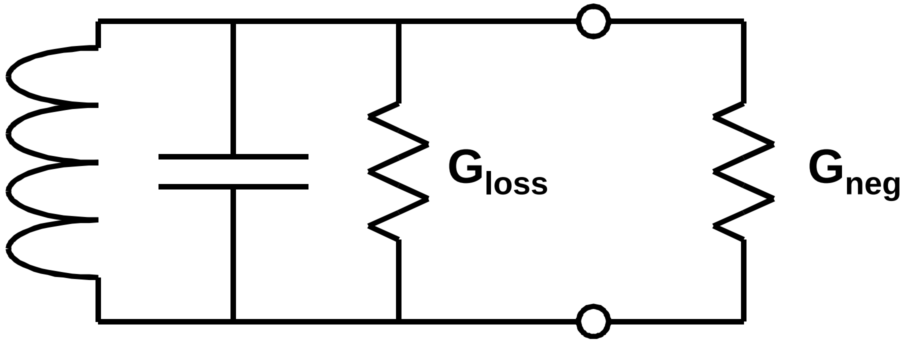



Real implementation is differential and simple cross-coupling creates proper fb.

+ can be transistor-only circuit
  → small area
+ Easy to tune, large tuning range

💣 power cons. is relative to freq.
  (although follows technology-nodes)
💣moderate (poor) phase noise

# LC Oscillator

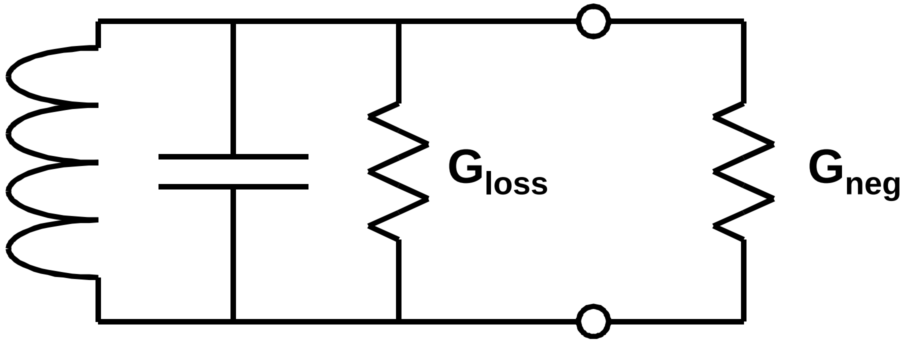



$$\omega_{osc} = \sqrt{\frac{1}{LC}}$$

$$G_{loss} - G_{neg} \leq 0$$

Is negative resistor a plausible device at all?

# LC Oscillator

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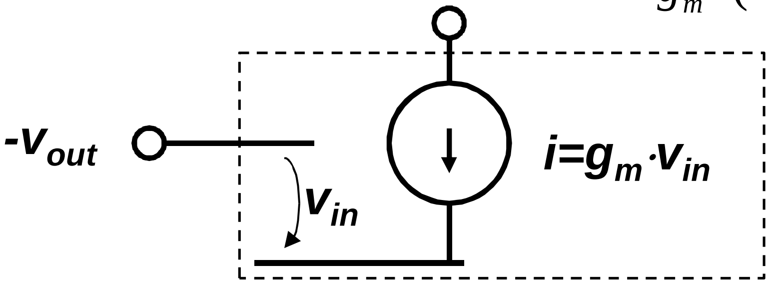
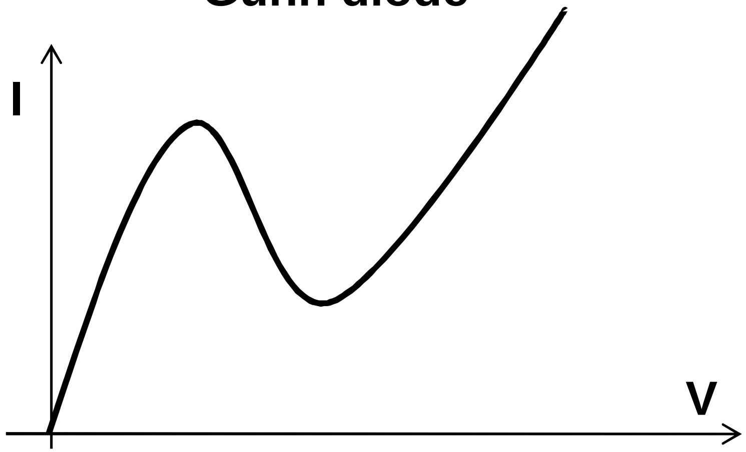
Is negative resistor a plausible device at all?

**Transconductor in unity feedback**



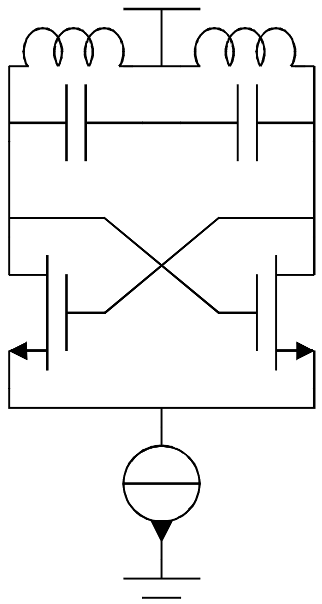

$$R_{in} = \frac{v_{out}}{g_m \cdot (-v_{out})}$$

**Gunn diode**



# Negative Conductance : Unity Feedback

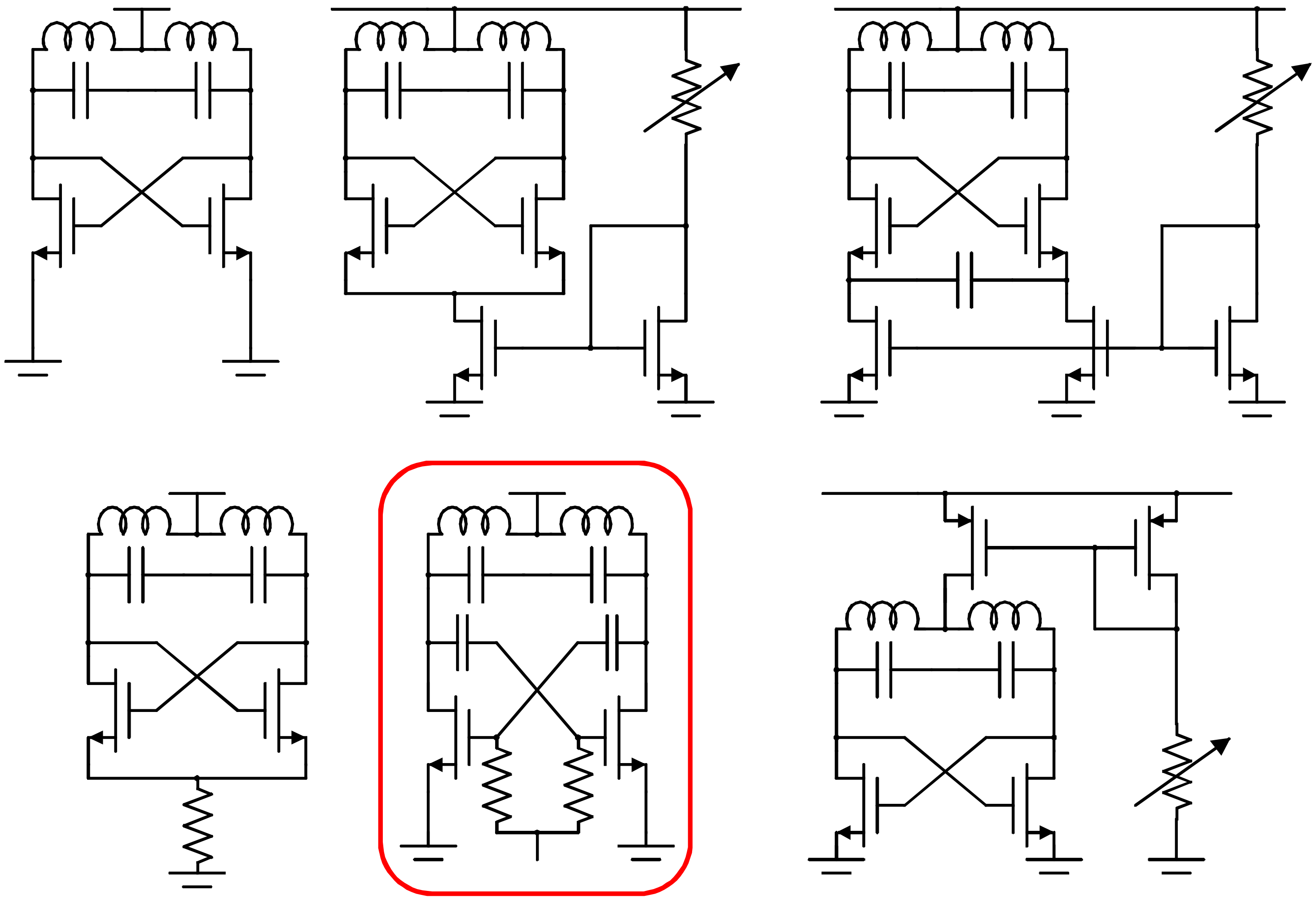
(most of modern RFIC VCOs use these)



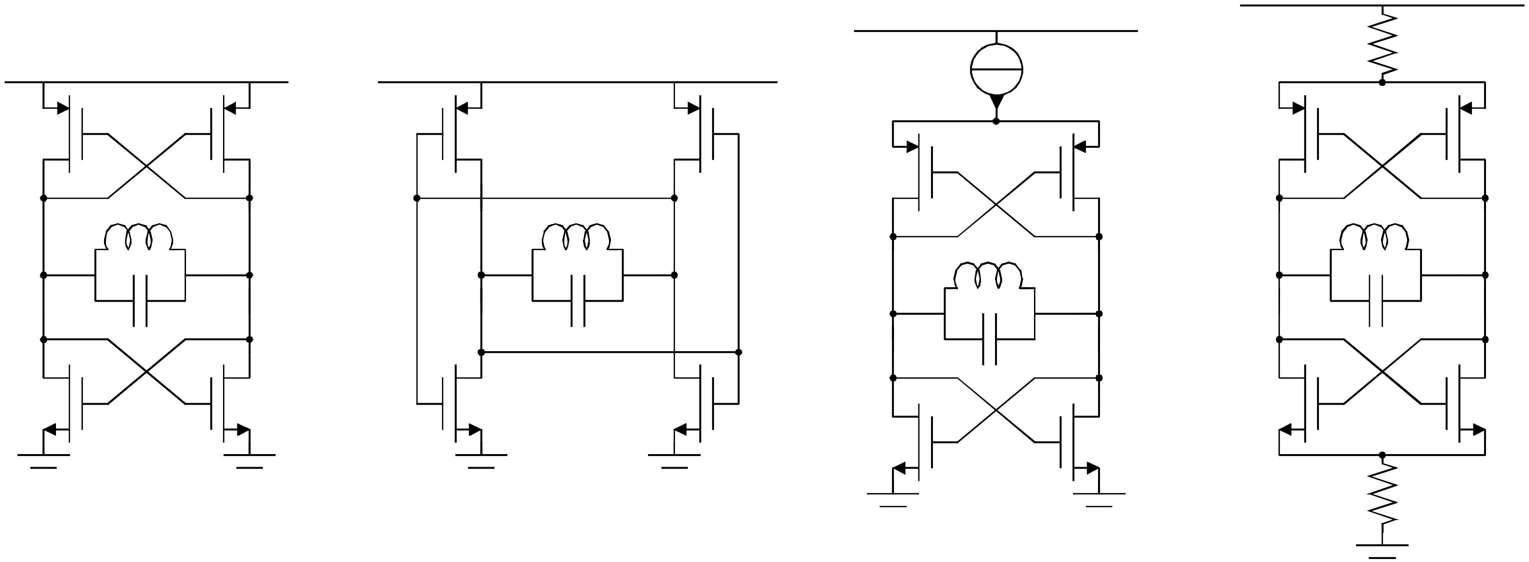
- Cross-coupled pair (CCP) :  NMOS / PMOS / CMOS
- Biasing : top / bottom / none
- Advanced techniques like noise filtering

  → Really many different topologies exist

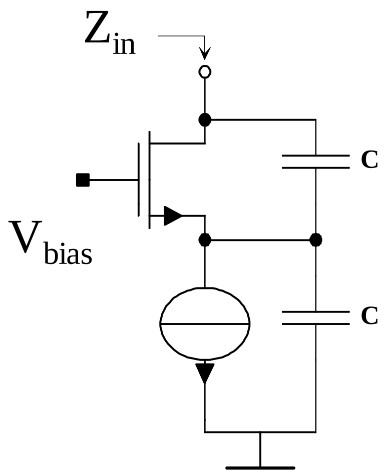
# NMOS CCP Biasing



# CMOS Cross-Coupled Pair



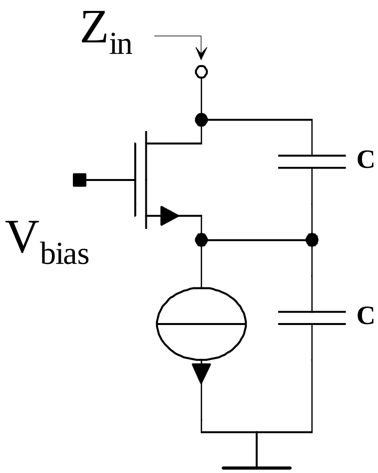
# Negative conductance : reactive feedback




nmos = $g_m$ and $V_{bias}$–node is signal ground

$$Z_{in} = -\frac{g_m}{\omega^2 C^2} + \frac{1}{j\omega \frac{C}{2}}$$

# Negative conductance : reactive feedback

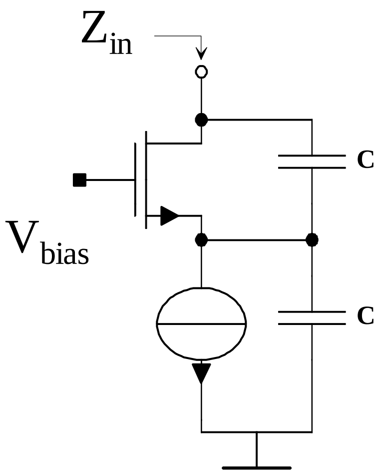



nmos = $g_m$ and $V_{bias}$–node is signal ground

$$Z_{in} = -\frac{g_m}{\omega^2 C^2} + \frac{1}{j\omega \frac{C}{2}} + \left(R_{coil} + j\omega L\right)$$

Add a coil → oscillator

# Negative conductance : reactive feedback

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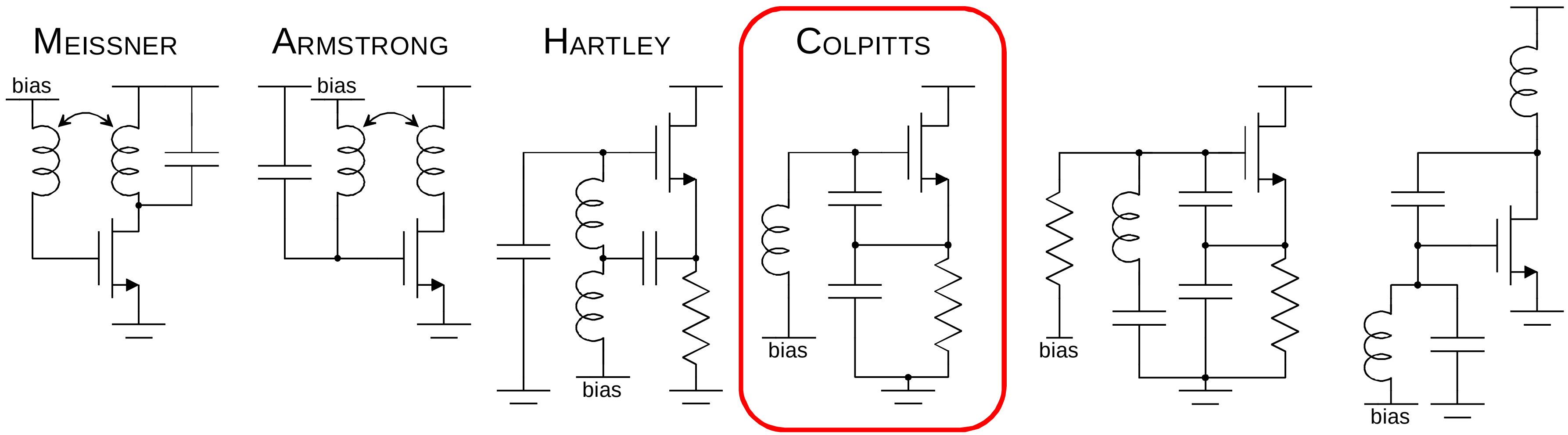
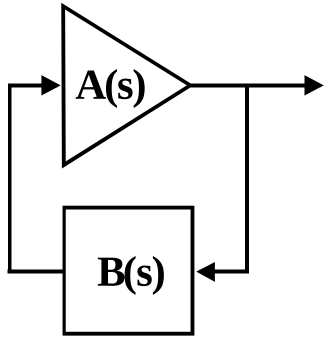
Some Classical Oscillators



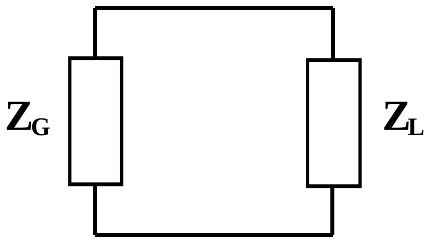
# Linear Analysis Methods

1) **Loop-Gain**




$$|A(j\omega_{osc})B(j\omega_{osc})| \geq 1$$
$$\angle A(j\omega_{osc})B(j\omega_{osc}) = 180^{\circ}$$

2) **Negative-Resistance**




$$R = R_G(\omega_0) + R_L(\omega_0) \leq 0$$
$$X = X_G(\omega_0) + X_L(\omega_0) = 0$$

3) **Nodal Equation**

See details:
L. Larson : RF and microwave circuit design for wireless communications

$$[Y]\cdot[V] = 0 \;\Rightarrow\; |Y| = 0 \;\Rightarrow\; RE\{|Y|\} = 0$$
$$IM\{|Y|\} = 0$$

in each case you get two equations
one for $f_{osc}$ and second for $-g_m$

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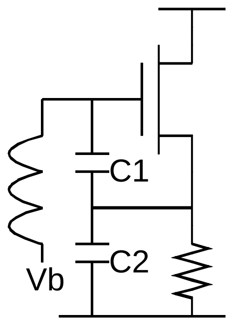
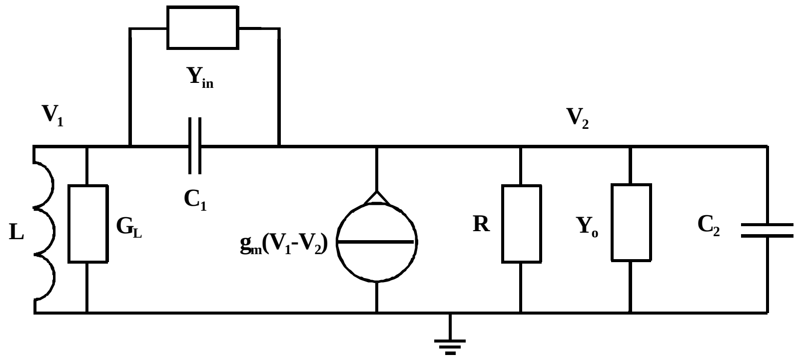
# Example: Common-Drain Colpitts




$$\begin{vmatrix} \frac{1}{j\omega L}+Y_{in}+j\omega C_1+G_L & -Y_{in}-j\omega C_1 \\ -Y_{in}-j\omega C_1-g_m & j\omega(C_1+C_2)+Y_{in}+\frac{1}{R}+Y_o+g_m \end{vmatrix}=0$$

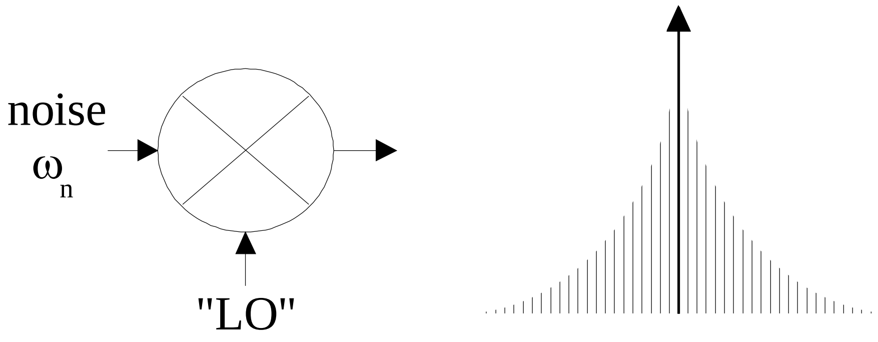
$$\omega=\sqrt{\frac{1}{L\frac{C_2\left(C_1+C_{in}\right)}{C_1+C_2+C_{in}}}+\frac{G_L\left(\frac{1}{R}+g_o+g_m\right)}{C_2\left(C_1+C_{in}\right)}}$$

$$g_m>\frac{C_1+C_{in}}{C_2}\left(\frac{1}{R}+g_o\right)+G_L\left(2+\frac{C_1+C_{in}}{C_2}+\frac{C_2}{C_1+C_{in}}\right)$$

# Oscillator Phase Noise

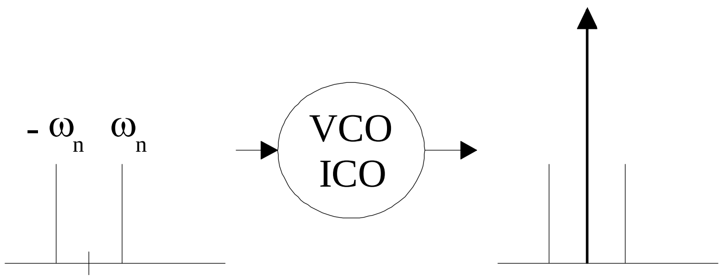
**Intuitive approach** : ”noise mixing”

- Oscillator is a nonlinear circuit
- oscillation swing is ”internal LO”
- noise (int. & ext.) is mixed into carrier
- fb-loop performs filtering




**Intuitive approach II** : ”Frequency modulation”

- Oscillator is a VCO & ICO
- noise is modulating the oscillator frequency




Narrowband FM approximation

$$v_{osc}(t) \approx A\cos\omega_0 t + \frac{A \cdot V_m \cdot K_{VCO}}{2\omega_m}\left[\cos(\omega_0 + \omega_m)t - \cos(\omega_0 - \omega_m)t\right]$$

Low phase noise

→ Minimize nonlinearity

→ Minimize $K_{VCO}$ and other sensitivities

# Oscillator Phase Noise

Consider ideal parallel LCR-type oscillator with noiseless $G_{neg}$.

There are losses in the resonator and corresponding noise source is $\frac{\overline{i_n^2}}{\Delta f} = 4kTG$

Impedance of the LC-tank $Z(\omega_0 + \Delta\omega) \approx -j \frac{\omega_0 L}{2\frac{\Delta\omega}{\omega_0}}$

Tank quality factor $Q = \frac{1}{\omega_0 LG} \Rightarrow L = \frac{1}{\omega_0 QG}$

We have $\left|Z(\omega_0 + \Delta\omega)\right| \approx \frac{\omega_0}{2\frac{\Delta\omega}{\omega_0}\omega_0 QG} = \frac{1}{2QG}\frac{\omega_0}{\Delta\omega}$

Noise voltage is $\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} \cdot |Z|^2 = 4kTR\left(\frac{1}{2Q}\frac{\omega_0}{\Delta\omega}\right)^2$

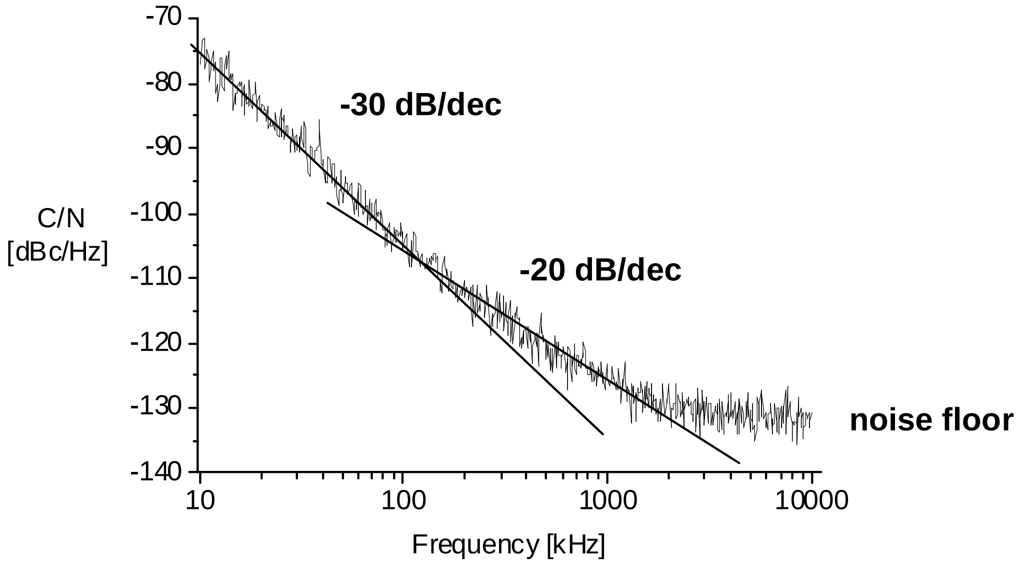
This is both amplitude and phase noise. Oscillator performs amplitude clipping → no amplitude noise. Thus, divide above by two. Also recall $\overline{v_{sig}^2} = P_{sig} \cdot R$

Noise-to-carrier ratio is

$$\boxed{N/C = \frac{2kT}{P_{sig}}\left(\frac{1}{2Q}\frac{\omega_0}{\Delta\omega}\right)^2}$$

Low phase noise
→ Maximize $P_{sig}$ and Q

# Leeson's Phase Noise Model




$$L(\Delta\omega) = 10 \cdot \log\left\{ \frac{2kT \cdot F}{P_{sig}} \left(1 + \left(\frac{1}{2Q}\frac{\omega_0}{\Delta\omega}\right)^2\right) \cdot \left(1 + \frac{f_c}{\Delta\omega}\right) \right\}$$

Heurestical model (based on experiments)

- $f_c$ is 1/f-noise corner → close-in noise
- constant term ”1” is included to describe the noise floor
- F is for additional noise due to $-g_m$

- $f_c$ is not the same as device's 1/f-corner
- F is difficult to estimate *a priori*
- Based on linear time-invariant model

# Frequency Dividers

From RF designer's point of view there are two types of logic: dynamic & static

**Dynamic logic:**

- ”memory” element needs to be refreshed
- transistors operate as switches
- many logic families
- on/off switching → limited speed
- power consumption is related to speed :

$$P_{DC} = f \cdot V_{dd}^2 \cdot C$$

- speed scales with the technology
- power consumption scales with the technology

**Static logic** (SCL = source-coupled logic)

- ”memory” element has continious current
- devices have constant bias (no saturation)
- no speed limitation (as with dyn. logic)
- power – frequency dependency weaker
- differential signals (dyn. logic single-ended)

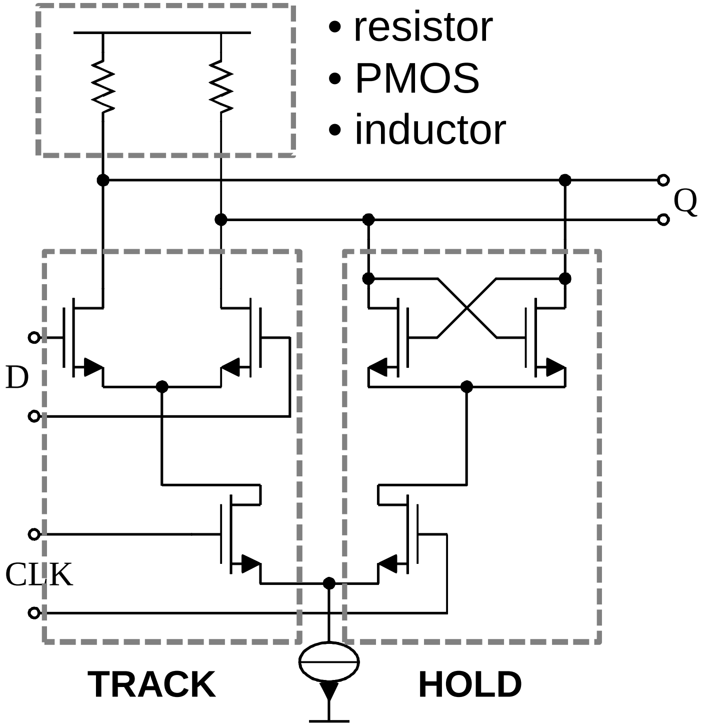
→ Better immunity to noise, glitches etc.

→ There is a frequency limit, set by the limited speed of dynamic logic or increased power consumption, where static logic becomes superior.

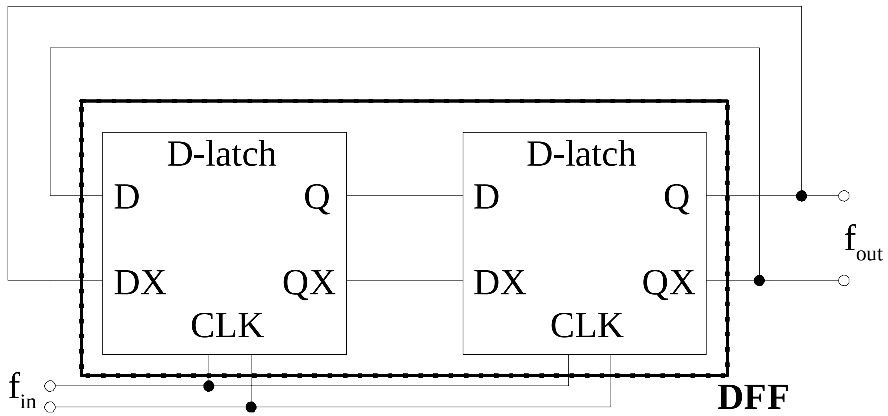
With 65-nm CMOS this limit is in range of 2-3 GHz, in 28-nm at 5-7 GHz.

# SCL D-flipflop divider

- D-flipflop in unity feedback is a divide-by-two circuit
- D-flipflop consists of two D-latches

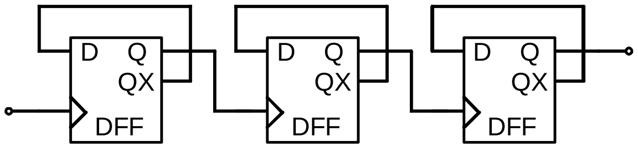



- resistor
- PMOS
- inductor



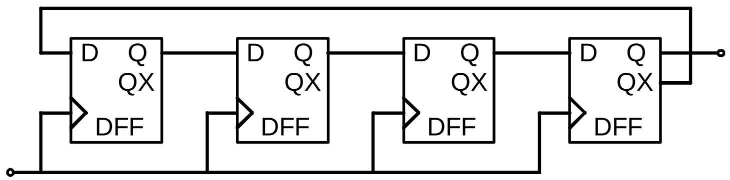
# Divider Chains

**Asynchronous chain**
Divide by **$2^N$**




- Power consumption lower after each division
- Higher noise (jitter)

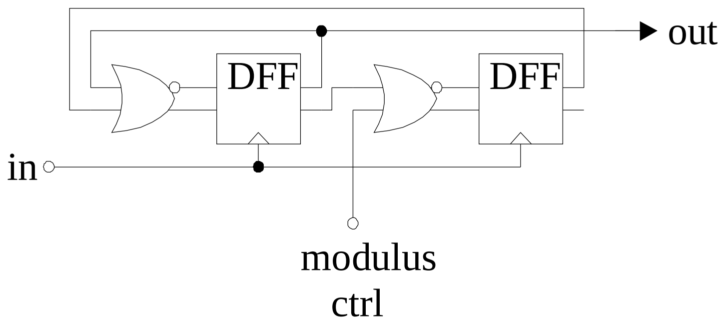
**Johnson counter**
Divide by **2N**



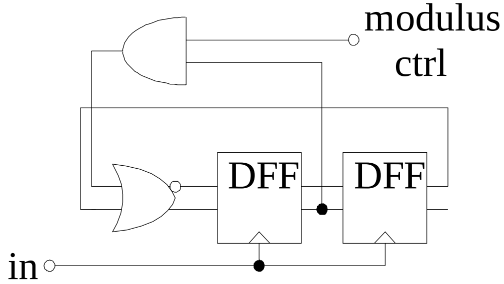

- Each DFF runs at $f_{in}$ →higher power cons.
- smaller noise (jitter)

**Dual-modulus dividers**

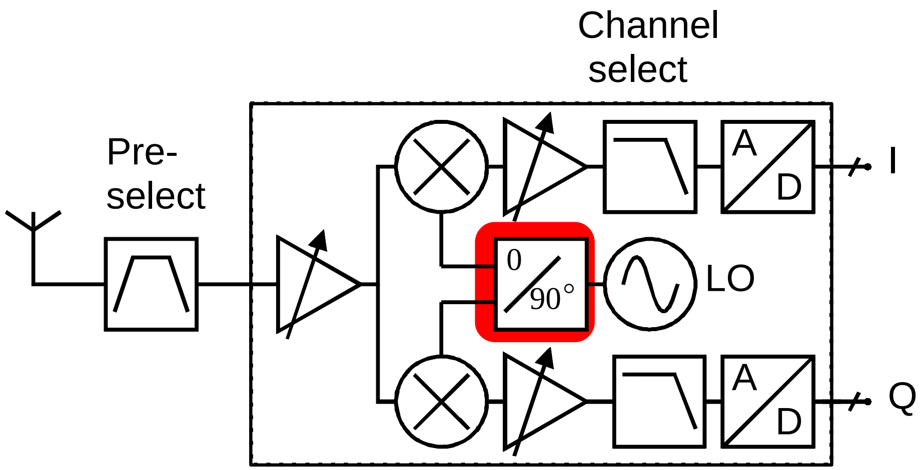
**Div-2/3**




**Div-3/4**



# IQ Generation

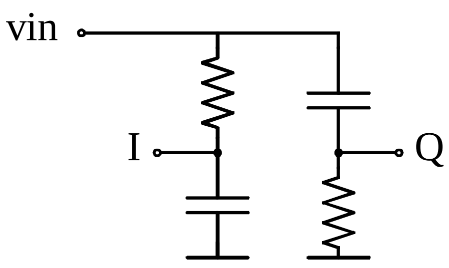



Four LO signals needed:
0° / 90° / 180° / 270°

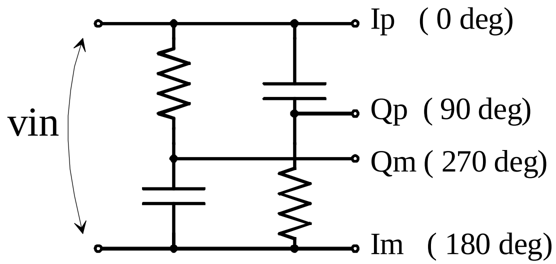
IQ amplitude and phase
balance (IRR) very important.

1. RC phase shifters → polyphase RC filter
2. Divide-by-two circuit
3. Quadrature oscillators

# RC Phase Shifters




constant IQ phase balance

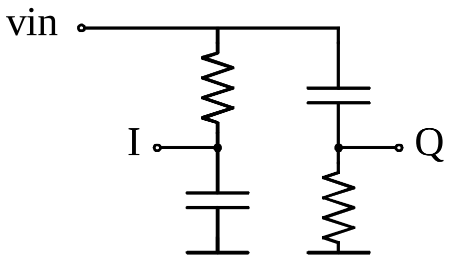



constant IQ amplitude balance

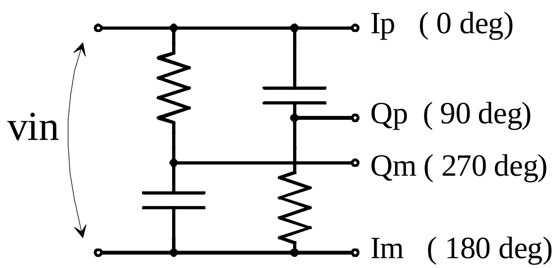
RC-CR network

- Narrow bandwidth
- Sensitive to process spread
- Post-tuning possible
- Clipping amplifier helps

# RC Phase Shifters




constant IQ phase balance




constant IQ amplitude balance

RC-CR network

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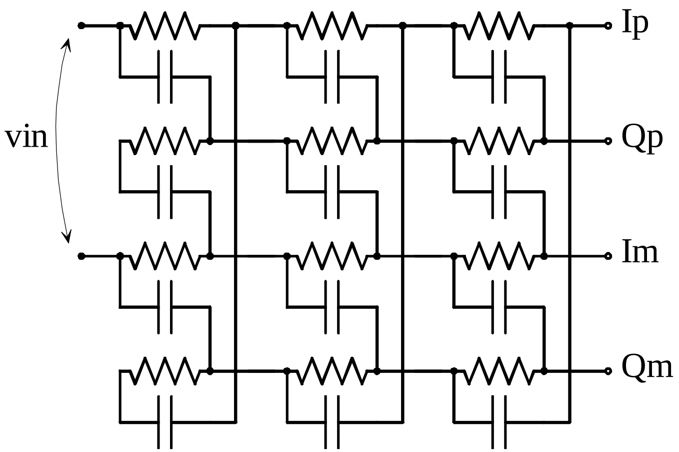
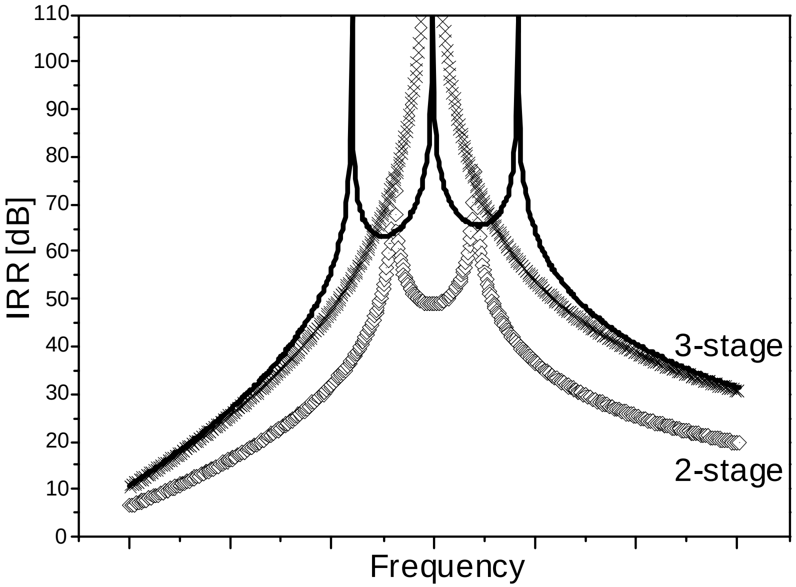
- Clipping amplifier helps

## Polyphase RC filter



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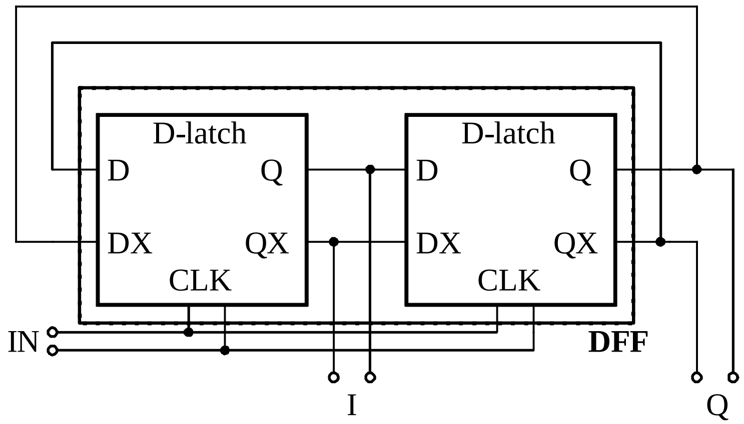
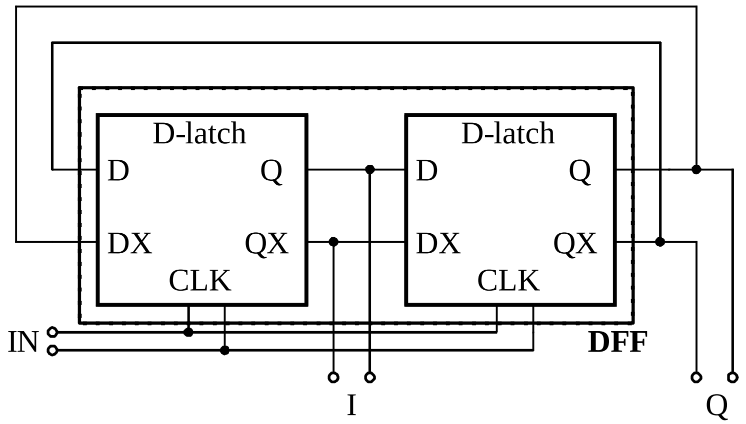
# Divide-by-two IQ Generation




- Wide bandwidth
- Compact size, easy to design well
- IRR limited by latch matching
- Requires double-freq signal
- Non-perfect input signal:
  - Amplitude error => phase error
  - Phase error attenuates a bit

# Divide-by-two IQ Generation

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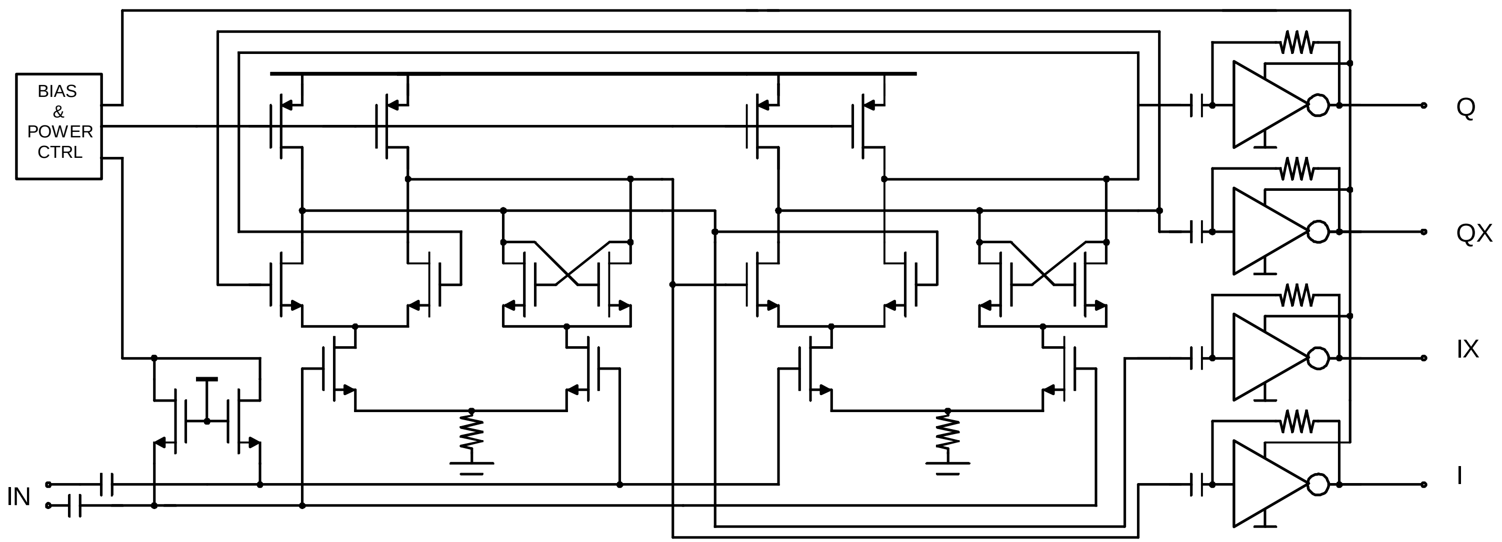
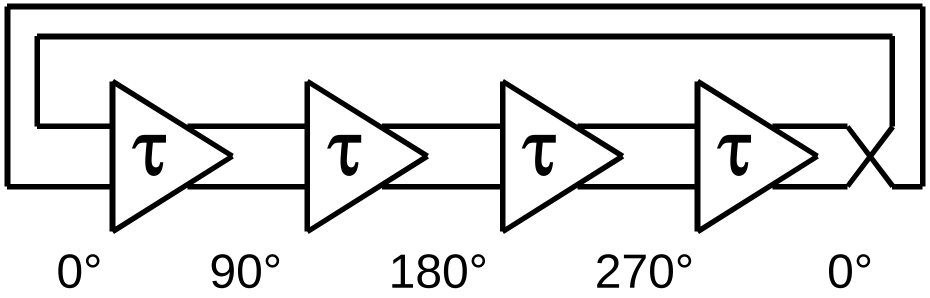
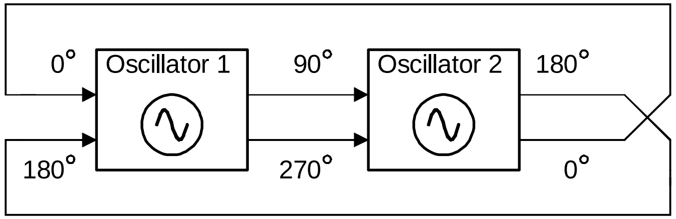
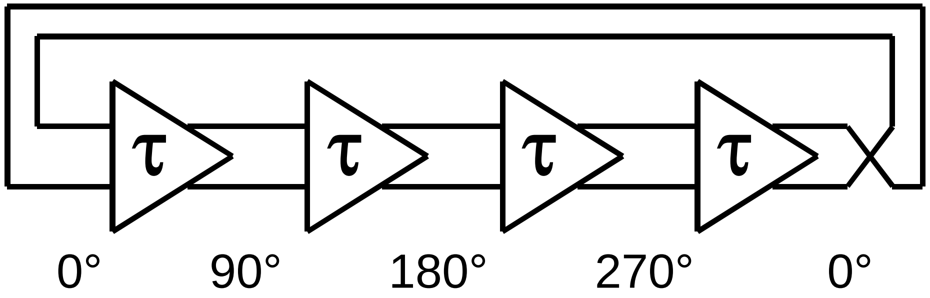


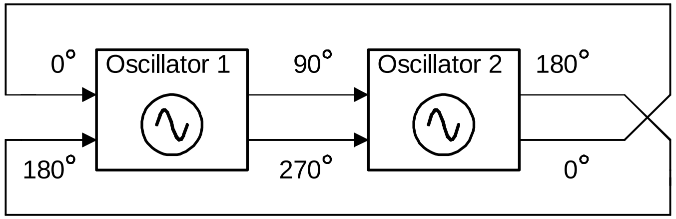
# Quadrature Oscillators

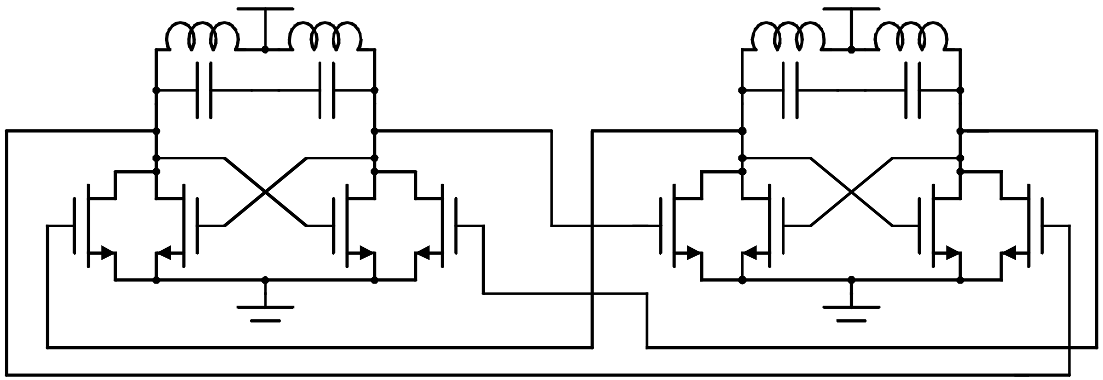


# Quadrature Oscillators



- Quadrature coupling results in increased phase noise
- Large die area



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# Summary

- SX requirements, impact of phase noise, IQ imbalance (IRR)
- DAS /  DDS  /  PLL
- CP-PLL
- ADPLL

- Oscillators: Ring & LC
  - LC-oscillators: unity feedback / reactive feedback
  - Phase noise
- Frequency Dividers: dynamic ”CMOS” / static ”SCL”
- IQ signal generation: RC polyphase / Div-2 / quadrature osc.