Project work is an essential part of the RF IC course. You will learn how to design CMOS RF IC circuit using a modern CMOS process and industrial-level design environment. The topic of the project work is an RF front-end for a GNSS receiver. Your task is to design the RF segment of such a receiver. Emphasize low power consumption and low die area in your design while still meeting the defined specifications.

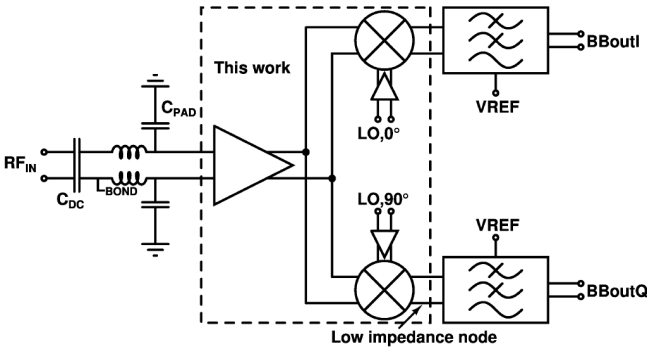

Figure 1. Block level details of the project work.

GNSS in brief:

Global navigation satellite systems (GNSS) have already become consumer level products, and many fascinating new applications, such as driverless vehicles, have been envisioned. U.S. system GPS is well-known, but also other systems are active or will be ready soon. GLONASS is the Russian system and COMPASS (BeiDou) the Chinese. European Union is building up its system, GALILEO, and it is planned to be fully functional with 30 satellites in orbit by 2019. GALILEO will be interoperable with GPS, i.e., it will use same carrier frequencies, although modulation schemes differ. From RF IC engineering point of view this means that the same RF portion can be used, but the digital signal processing unit needs to support both systems. Simple sketch of a GNSS receiver is shown below.

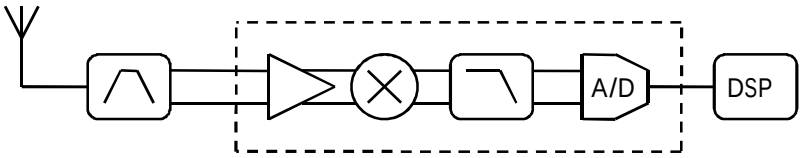

Figure 2. GNSS receiver chain. Preselect filter block includes a SAW filter and single-to-differential conversion.

In this project work you will design a receiver circuit that operates at the main civil service band of GALILEO and GPS systems (L1 / E1) with center frequency of 1575.42 MHz and bandwidth support up to 20 MHz so that also the envisioned advanced modulation schemes can be supported. Furthermore, we take into account that an interfering cellular phone may operate at close vicinity. 2G/3G systems at 1710 MHz are the closest and therefore most harmful. Preselect filter will attenuate that signal by about 30 dB, but still interfering signals with significant power levels will enter the receiver. In general, a GNSS receiver needs to have very good sensitivity because the signals from the satellites are very weak and antennas are omnidirectional. Sensitivity level below -140 dBm is the target, while in 2G/3G cellular systems it is at least 30 dB higher. These aforementioned considerations provide some background for the circuit performance requirements that are given in the next page.

What to do

The circuit structure under study is shown in the upper corner of this page. We have simplified this project work with an assumption that all gain tuning will take place in the baseband segment, and it will be provided for you as an ideal element. In addition, the interface at RF input includes DC-decoupling capacitors, bond-wire inductances and pad capacitances. Your task is to design the RF

front-end part and use the given baseband segment as a well-defined load. Furthermore, LO signals will be taken from ideal sources and you need to just design a simple amplifier (one/two stages) to drive the LO ports. In other words, you may not take large power out of ideal sources, but instead consider how much power you need to consume to drive the LO ports of your mixers. Finally, the third issue that we will overlook is 1/f noise. This is one reason to sometimes favor low-IF receiver architecture in some GNSS applications, but we chose the direct-conversion architecture here since it is simpler. Below is a summary of design objectives.

- Circuits to be designed: LNA, mixer, LO buffer
- For proper input matching, you can modify bond-wire inductances within 1-5 nH and DC-decoupling capacitors within 1-10 pF. Pad capacitance is fixed.
- LO sources are ideal 0.1-V sinusoidal voltage sources (details in the ELDO example file).
- The baseband filter input is a low-impedance node (details in the ELDO example file).

We will provide you a simple example file, where this kind of receiver is simulated using ELDO. In that example all sub-units are intentionally very simple and use ideal components. Your task is to replace them with real circuit structures and design the overall receiver RF front-end.

The circuit should meet the following specifications:

Frequency	1575 ± 10 MHz (bandwidth = 20 MHz)
Voltage gain	100 dB (about 20-30 dB at RF and the rest at BB)
Gain ripple	< 1 dB (within the 20-MHz band, 1565-1585 MHz)
Noise figure	< 2 dB at 1575 MHz
Blocker IP_{1dB} @1710 MHz	> -15 dBm
Input matching (S_{11})	< -10 dB at 1.4-1.7 GHz
Supply voltage	1.5 V
Current cons.	minimize
Die area	minimize You do not need to draw the layout in this project work, but do consider the use of coils and large capacitors.

Practical Arrangements

1) The circuit will be designed using Cadence schematic editor and Eldo circuit simulator. The technology is Cadence generic process design kit that mimics a 45-nm RF CMOS process.

2) The design and simulation tools for the project run in the computing environment provided by the Department of Electronics and Nanoengineering (ELE). You are required to fill in an application form for a computer account (if you don't yet have one), which will give you access to a server called **VSPACE.** The connection to this machine can be made using SSH or NX Client. We recommend a freeware software **x2go**. (http://wiki.x2go.org)

3) **Presentation**: In the last meeting each person will give a brief (10-15 minutes) presentation. A slide set of about 10 slides is appropriate. Include at least

1. all the schematics with device dimensions, and DC currents and operating points.
2. Sufficient amount of simulation results.
3. A block diagram indicating your gain partitioning, and ICP & IIP3 values
4. A summary table of performance – compared to given specs.
5. Give some comments on power consumption and the use of coils and caps (sizes matters!)

Draw your schematics using a graphical program, such as inkscape. That results good quality figures. Furthermore, simulations results can be taken from ezwave, but pay attention on settings – figures have to be such that audience is able to read them easily. Matlab figures are of better quality.

4) **Files that you will find from VSPACE at /home/E3550/project_work_instructions**

- ELDO example files
- Instructions for NX Client and VSPACE-server
- Instructions for the Cadence and ELDO
- Instructions on how to make good figures for the final presentation

5) **IEEExplore**: you may simply apply the basic circuit structures presented in the lectures and CAD exercises to complete your receiver. HOWEVER, if you target for the best grades (4-5) we strongly recommend that you will search for good circuit ideas by yourself. IEEE's database (http://ieeexplore.ieee.org) is available from Aalto domain. Try to find relevant papers with "good" search words. The following journals and conferences are the main forums for RF IC development:

- Journal of Solid-State Circuits
- Transaction on Microwave Theory and Techniques
- International Solid-State Circuits Symposium (ISSCC)
- European Solid-State Circuits Conference (ESSCIRC)
- Radio Frequency Integrated Circuits Symposium (RFIC)

9) **Ask for Advice**: if you have a simple well-defined problem, send email to Mahwish Zahra and cc Kari Stadius (mahwish.zahra / kari.stadius @aalto.fi). If your challenge requires personal discussions, please contact Mahwish by email to arrange a personal meeting, preferably on Tuesdays between 10.00-12.00.

10) **CAD Exercises** : CAD exercises (CAD0 - CAD4) will introduce you on simulations of each sub-block. Furthermore, you will find an example file in the vspace server that will provide you some guidance on the simulation of the full receiver. Therefore, after completing the CAD exercises you will all the tools and skills to complete this project work.