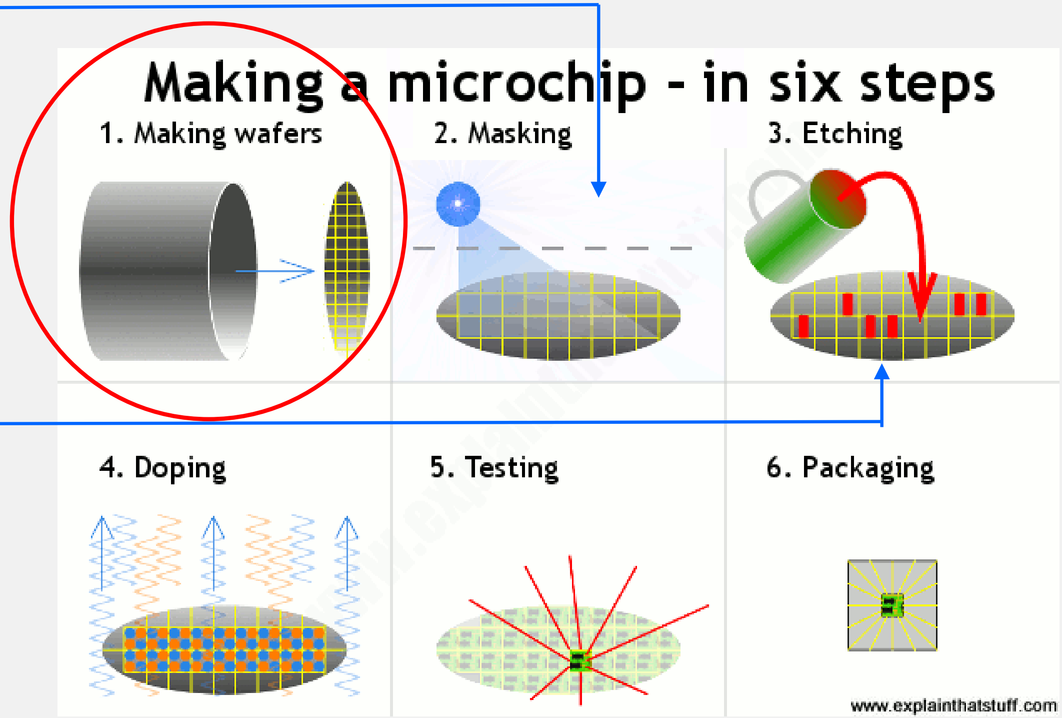
Silicon and Substrates

Victor Ovchinnikov

Chapters 4, 23.1, 25.4

Previous lecture

- Microfabrication
- Litho
- Etching



Outline

- Silicon unique status and properties
- Silicon growth and wafering
- Miller indices
- Defects
- Substrates

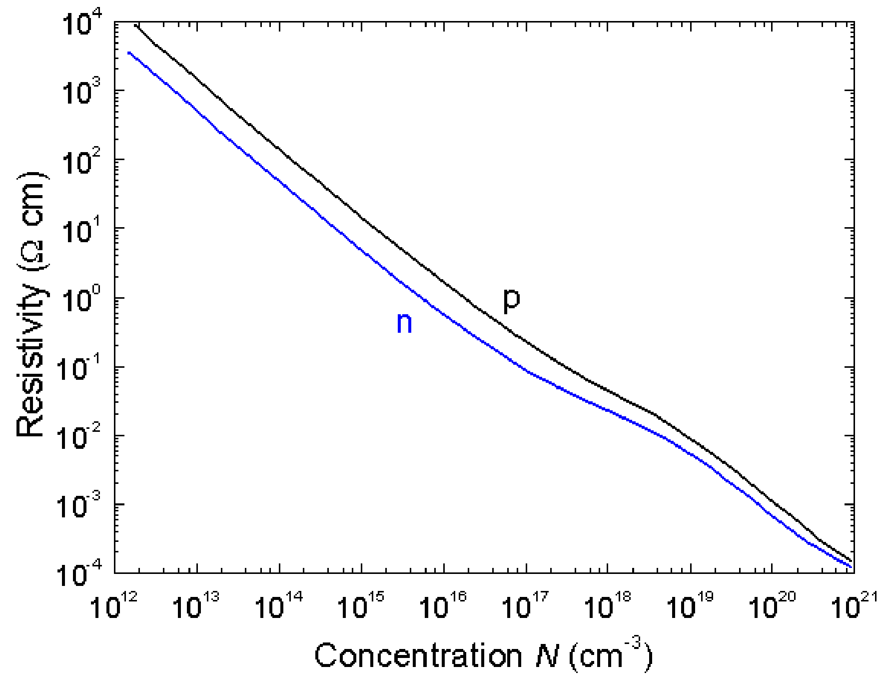
Natural silicon

$16 \times 26\ mm^2$

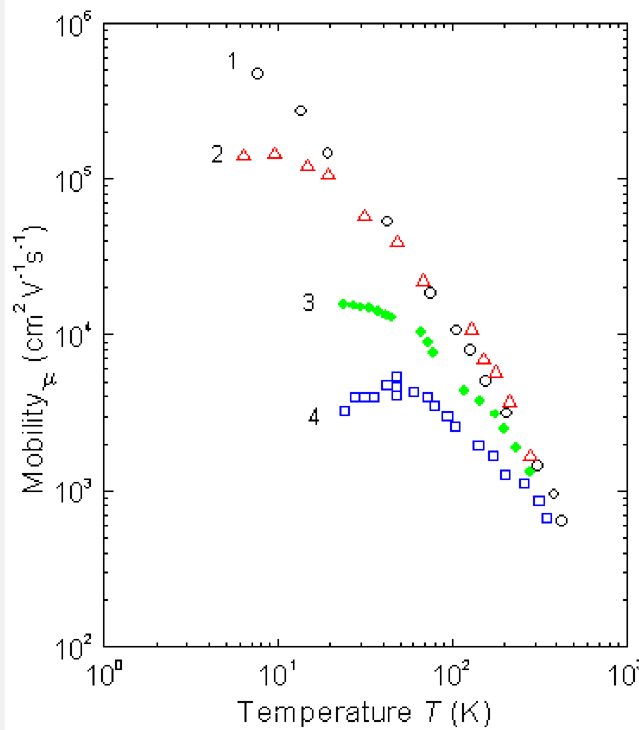
$32 \times 45\ mm^2$

Electronic properties

Resistivity

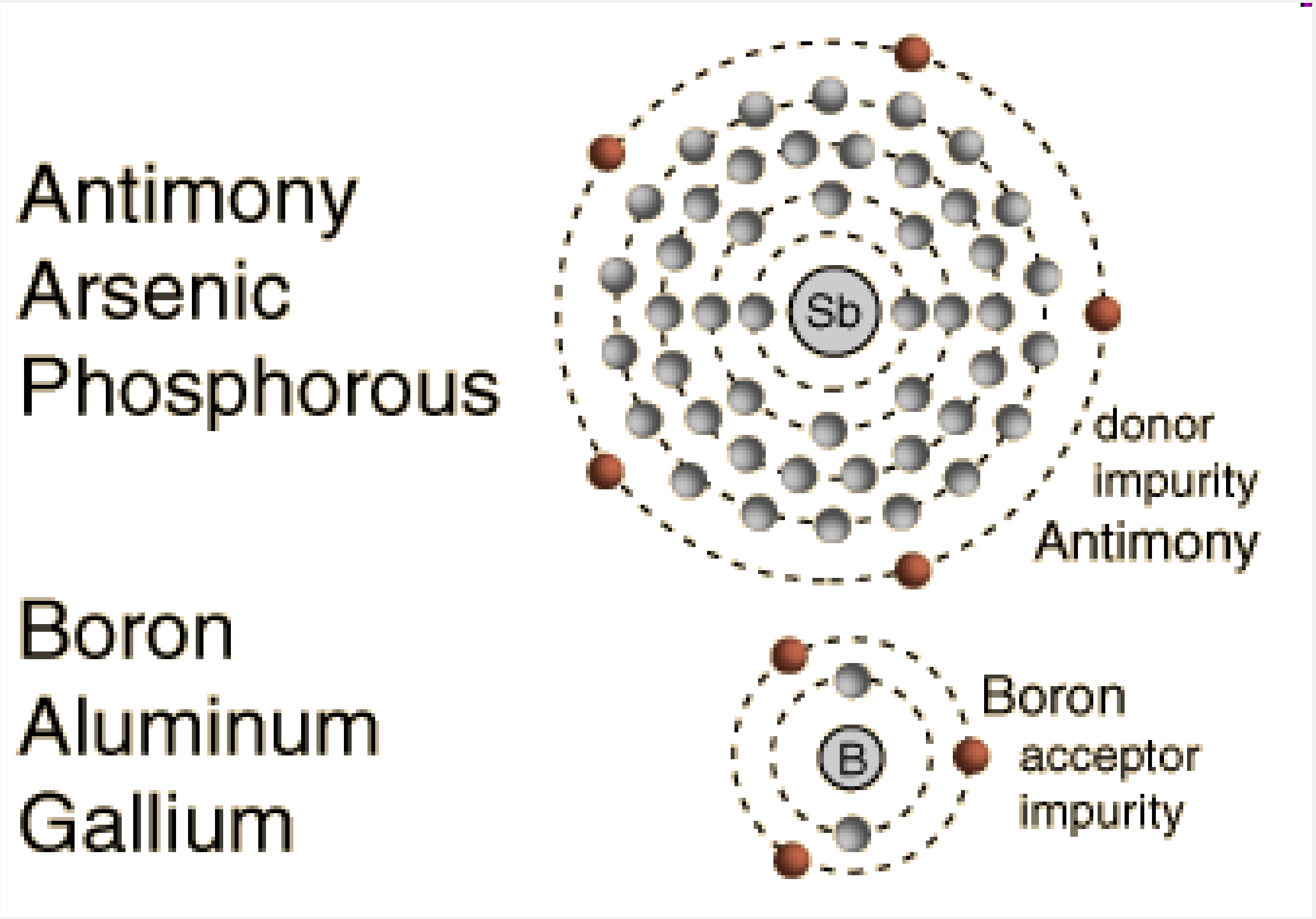


Mobility



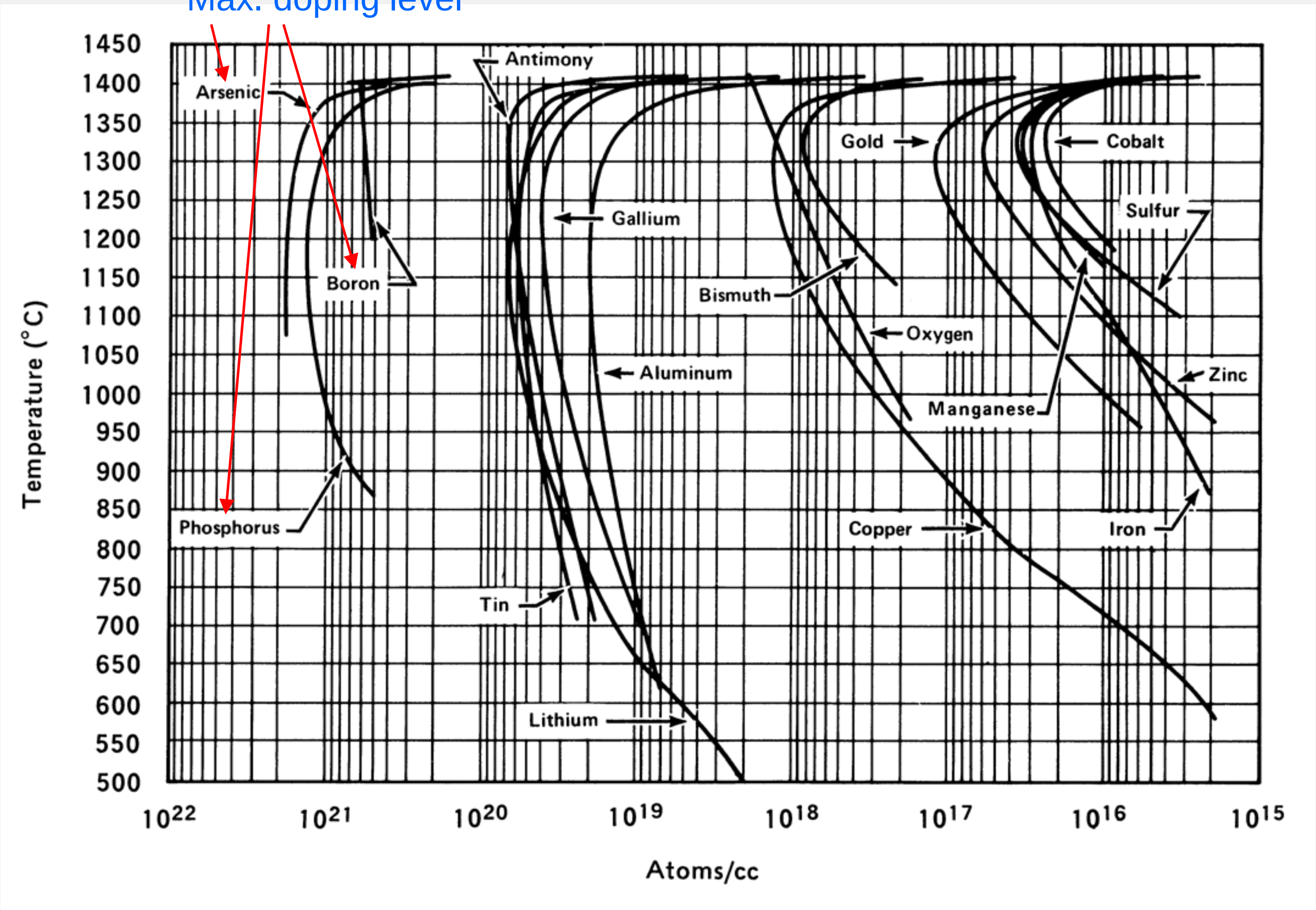
1. High purity Si (N_d< 10^{-12} cm^{-3}); time-of-flight technique (Canali *et al.* [1973])
2. High purity Si (N_d< $4 \cdot 10^{-13}$ cm^{-3}): photo-Hall effect (Norton *et al.* [1973])
3. N_d= $1.75 \cdot 10^{16}$ cm^{-3}; N_a = $1.48 \cdot 10^{15}$ cm^{-3}; Hall effect (Morin and Maita [1954])
4. N_d= $1.3 \cdot 10^{17}$ cm^{-3}; N_a = $2.2 \cdot 10^{15}$ cm^{-3}; Hall effect (Morin and Maita [1954])

Donors and acceptors for Si



Solid solubility – maximum dopant concentration in *c*-Si

Max. doping level

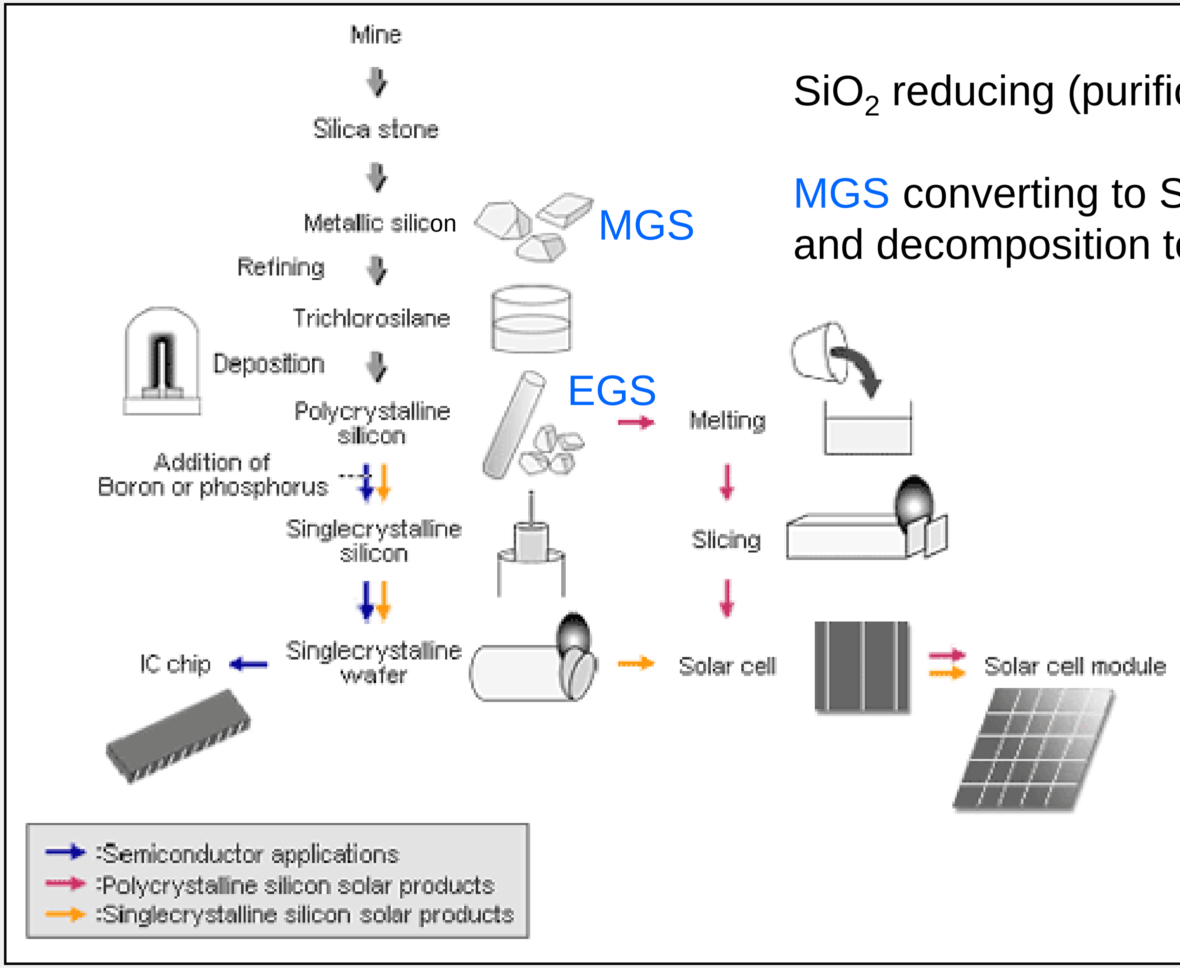


Types of doping

- Uniform doping
  - during crystal growth (doped raw Si)
  - during epitaxy - > lecture 8

- Selective doping - > lecture 8
  - by ion implantation
  - by diffusion

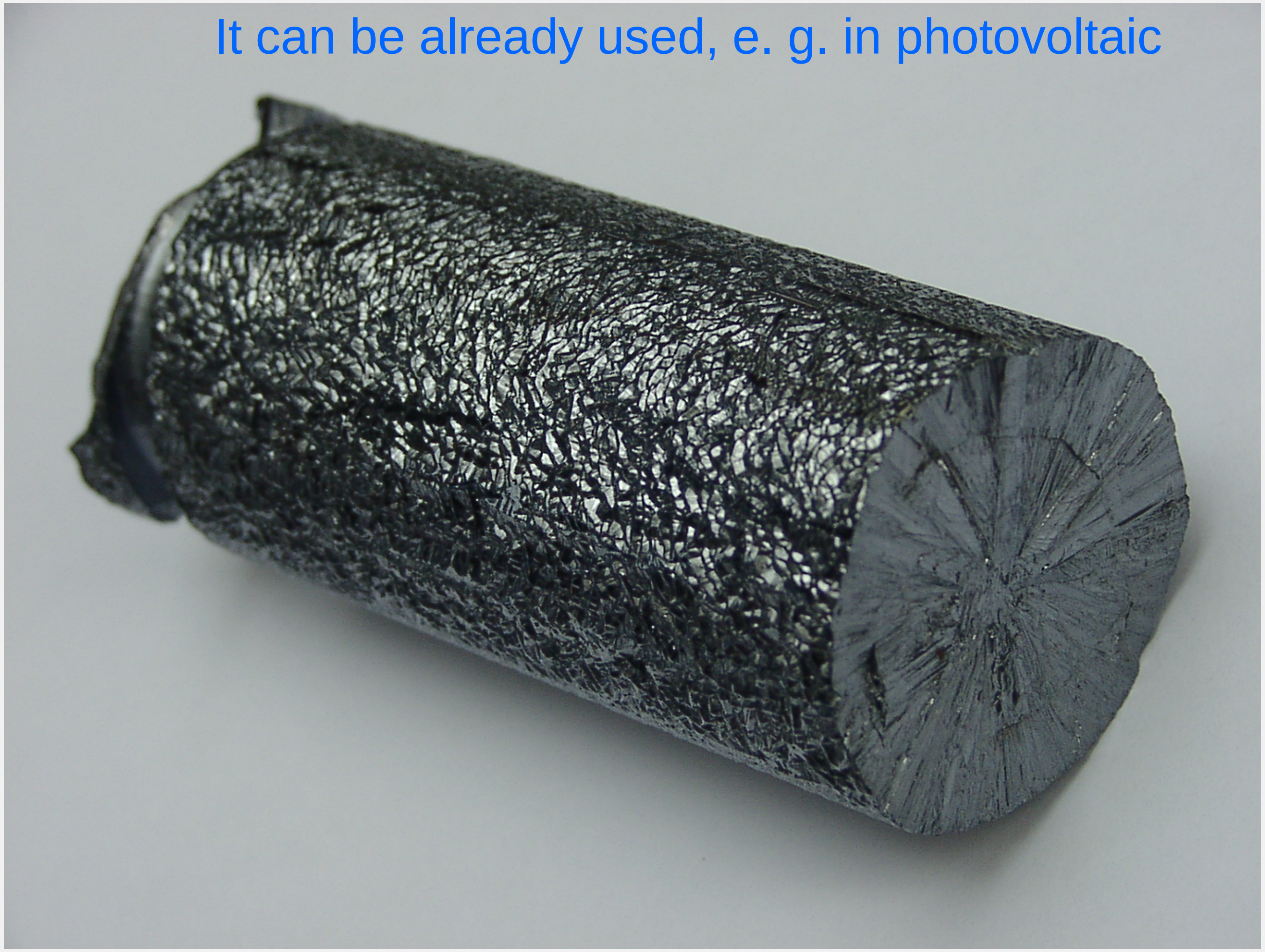
Si purification and production



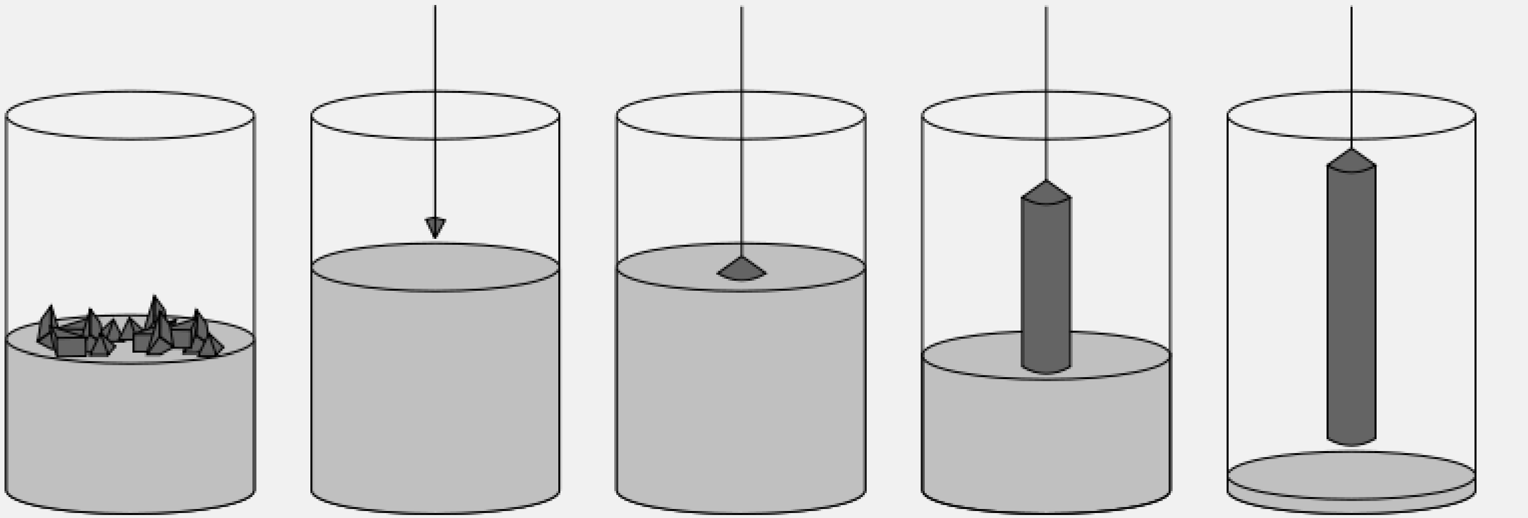
SiO_2 reducing (purification) -> MGS, 98% pure Si

MGS converting to $SiHCl_3$, distillation
and decomposition to Si -> EGS, ppb purity

EGS polysilicon



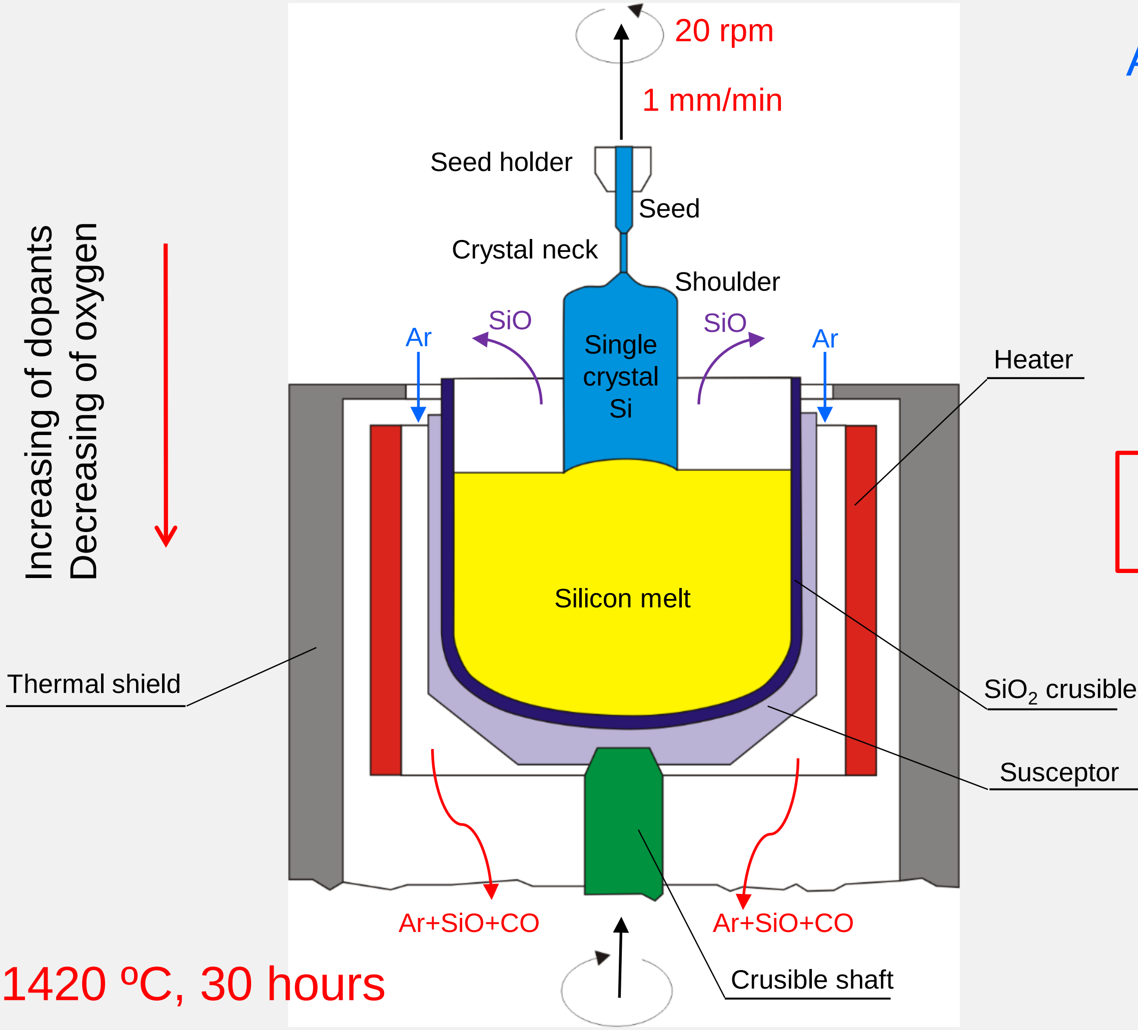
Czochralski crystal growth : liquid phase epitaxy



The method is 100 years old!

Czochralski (CZ) *c*-Si growth

Increasing of dopants
Decreasing of oxygen



1420 ºC, 30 hours

Always there is O_2 !

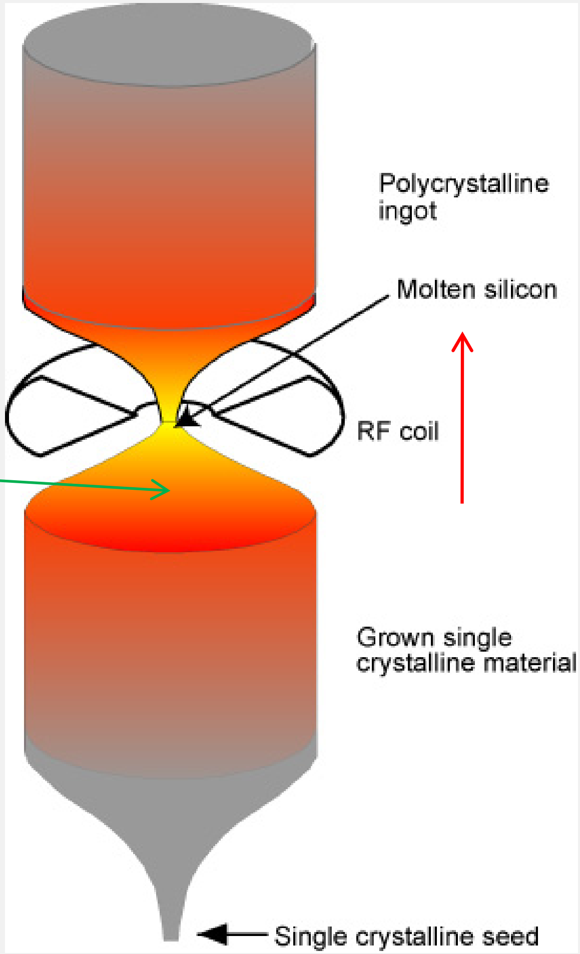
Segregation coefficient
$k_0 = C_{solid}/C_{liquid}$

Boron	0.8
Phosphorous	0.35
Oxygen	1.25
Carbon	0.07

1kΩ-cm – max resistivity

c-Si ingot

Float zone (FZ) growth



Impurities move with melted region

There is no O_2 !

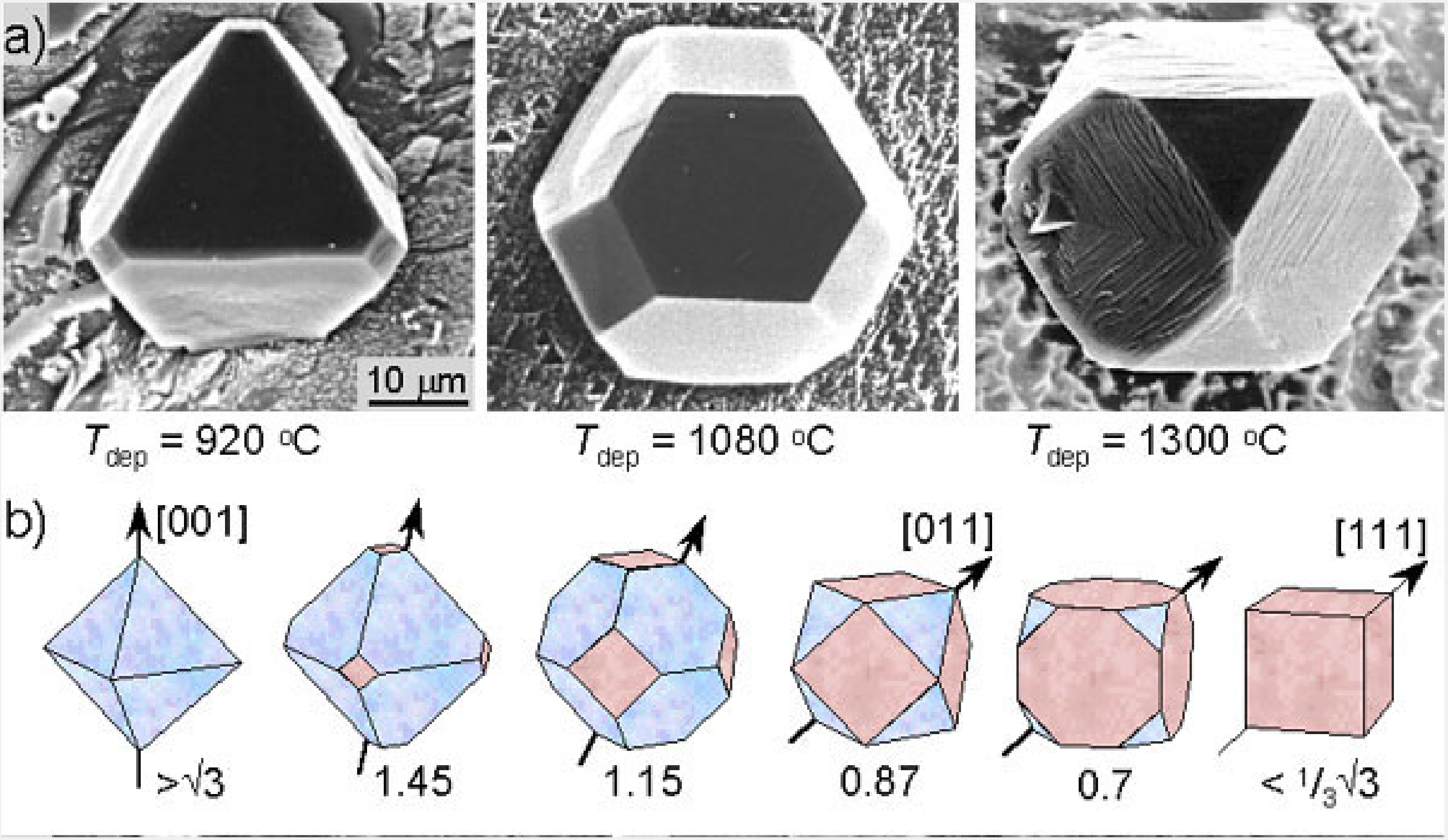
max 20kΩ-cm

max 150 mm (450 mm MCZ)

Vacuum or Ar ambient

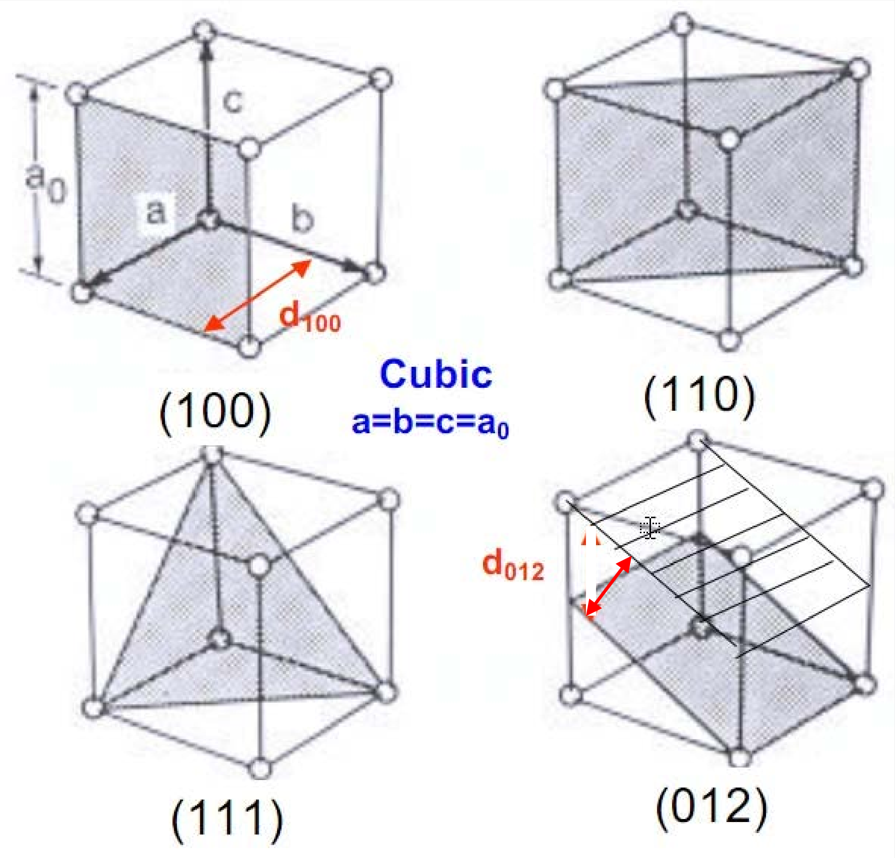
Crystal variety

Diamond shape variation



Si Miller indices

a	b	c
1	∞	∞
1	0	0



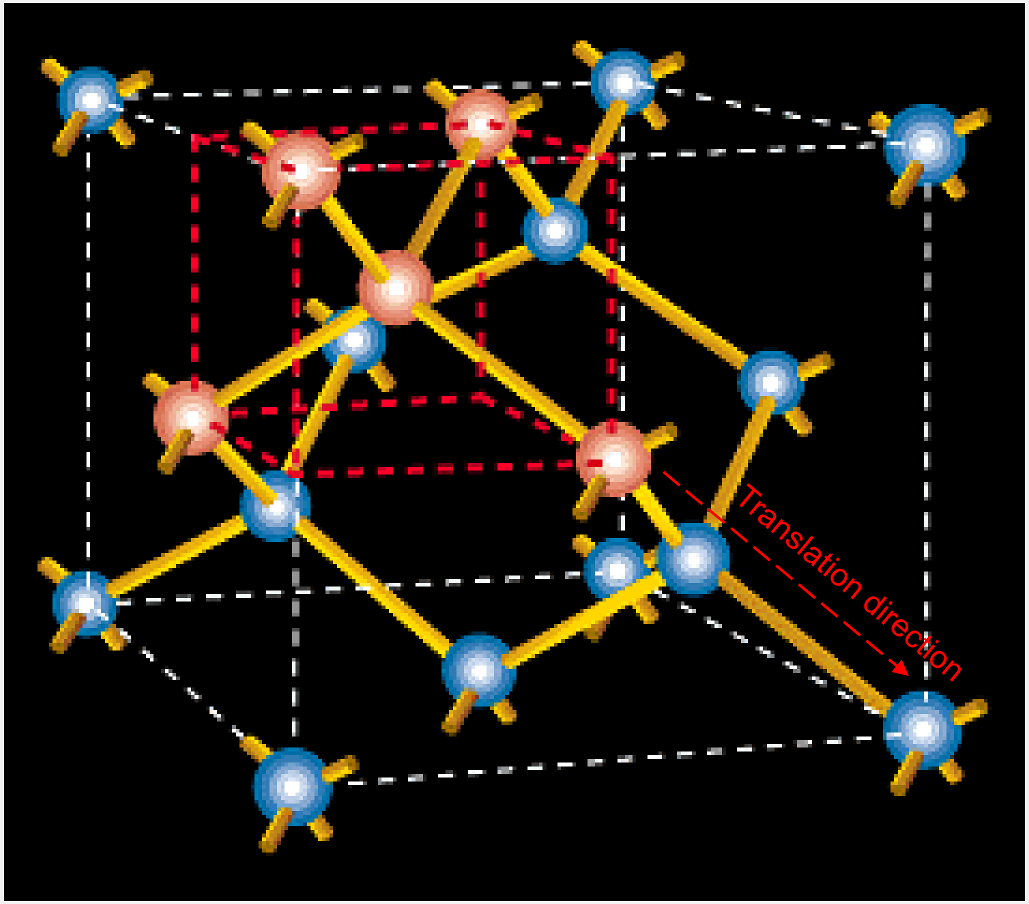
a	b	c
1	1	∞
1	1	0

a	b	c
1	1	1
1	1	1

a	b	c
∞	1	½
0	1	2

Black numbers-fractional intercepts, Blue numbers-Miller indices

Si unit cell



FCC or
"diamond cubic" lattice

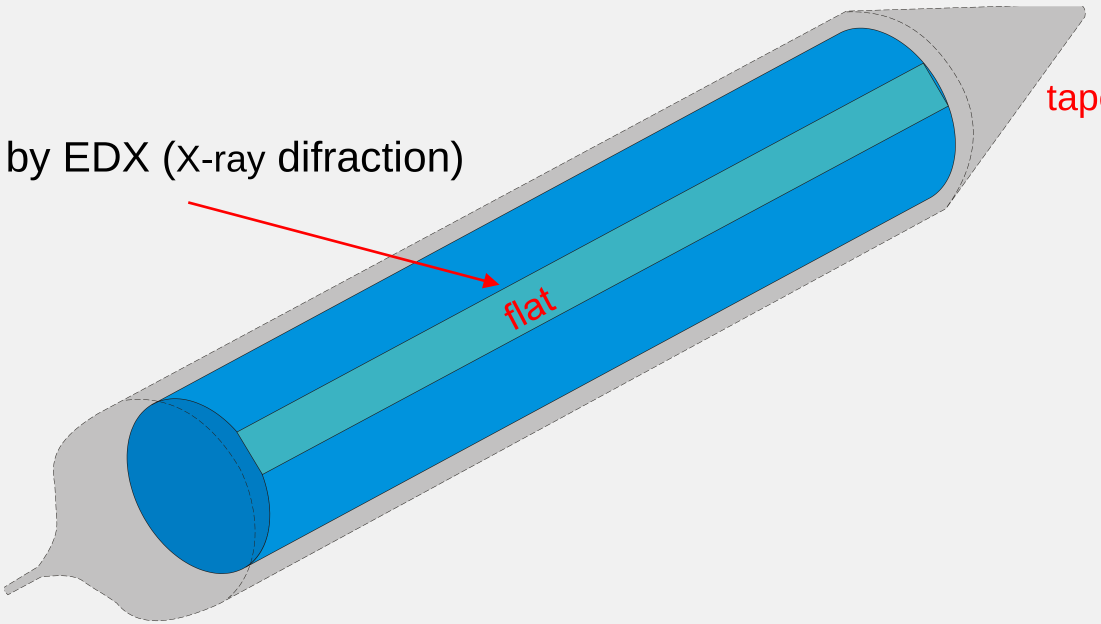
a=5.43Å

filled space 34%
(hexagonal 74%)

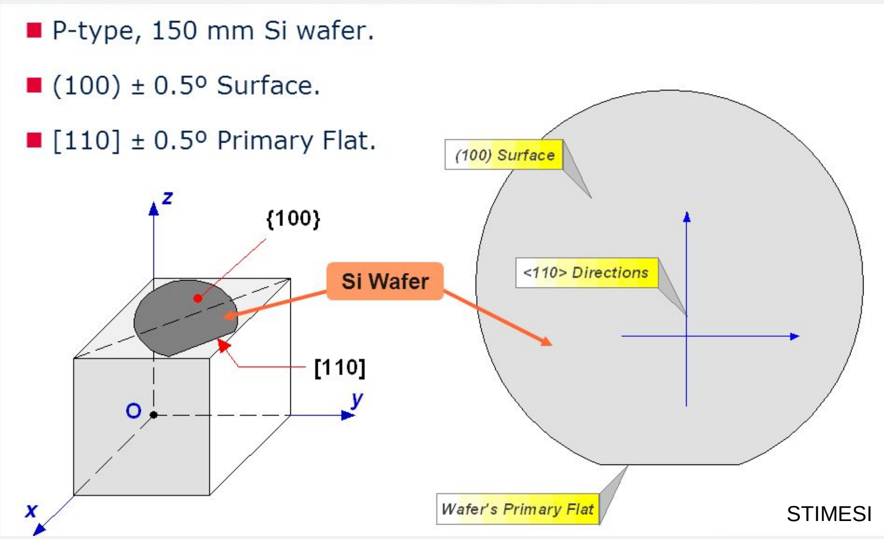
www-inst.eecs.berkeley.edu/~ee130/sp07

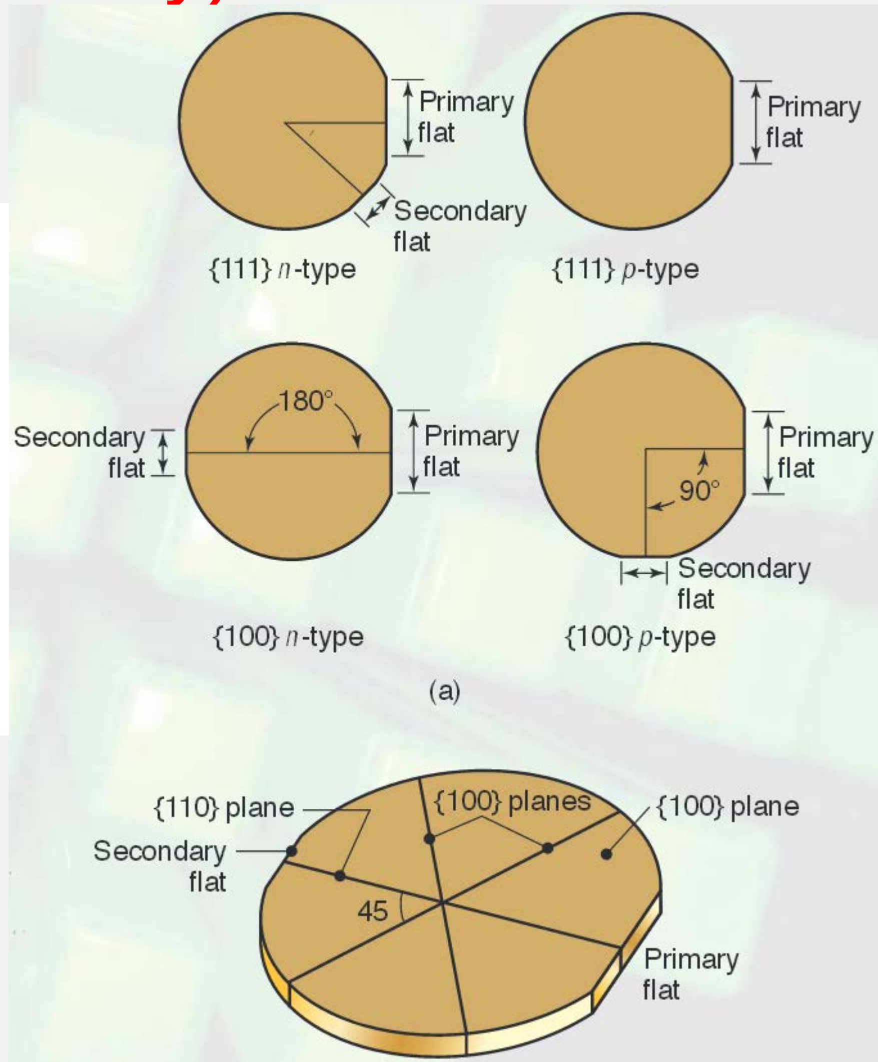
Crystal shaping

Flat is found by EDX (X-ray difraction)

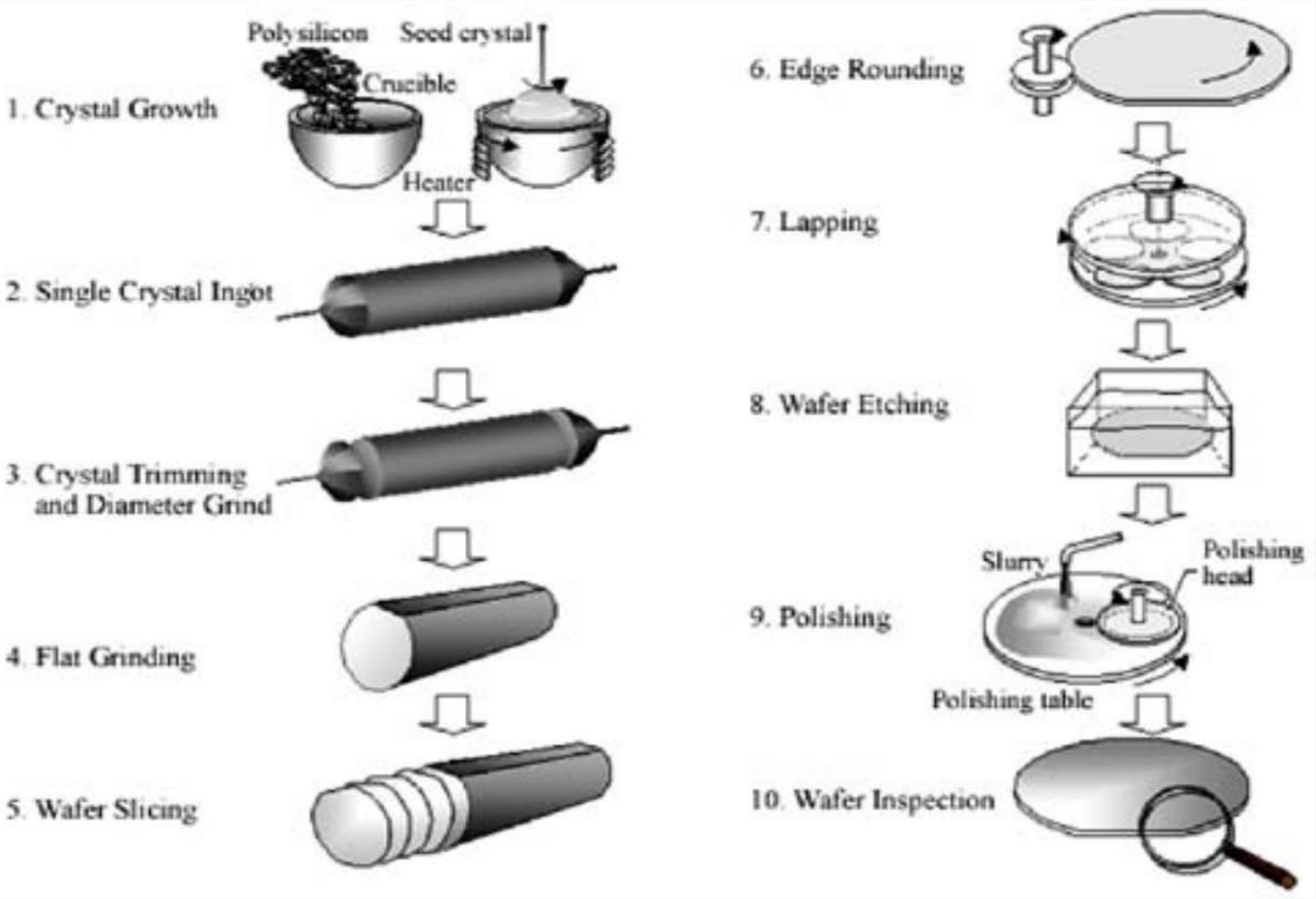


Base (primary) flat





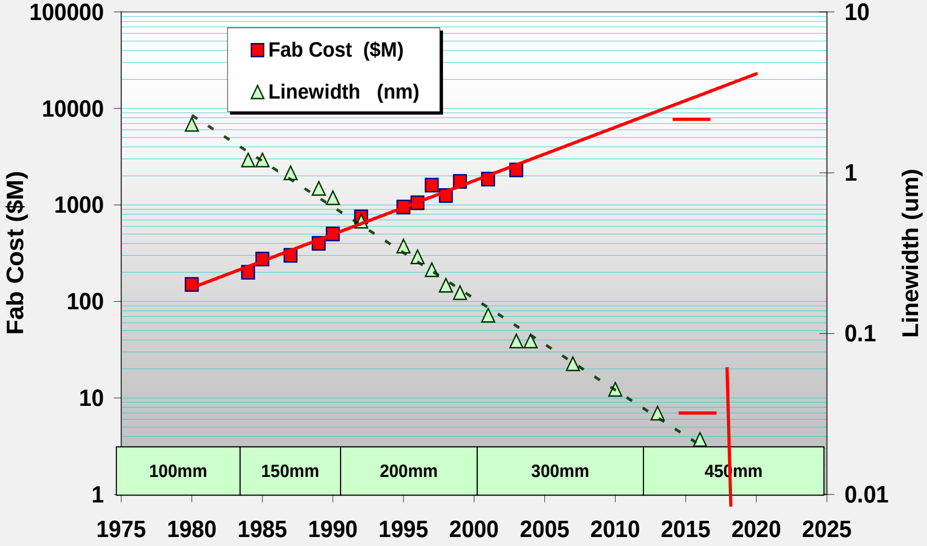
Silicon wafering



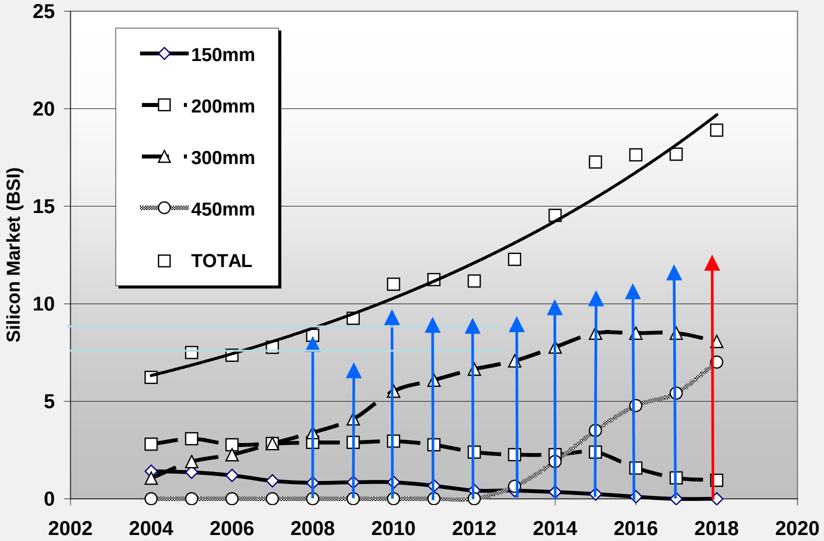
http://www.southalabama.edu/engineering/ece/faculty/akhan/Courses/EE539-Fall04/Lecture-slides/lecture-4-crystal%20growth.pdf

Forecasts and trends

Evolution of fab cost and wafer size

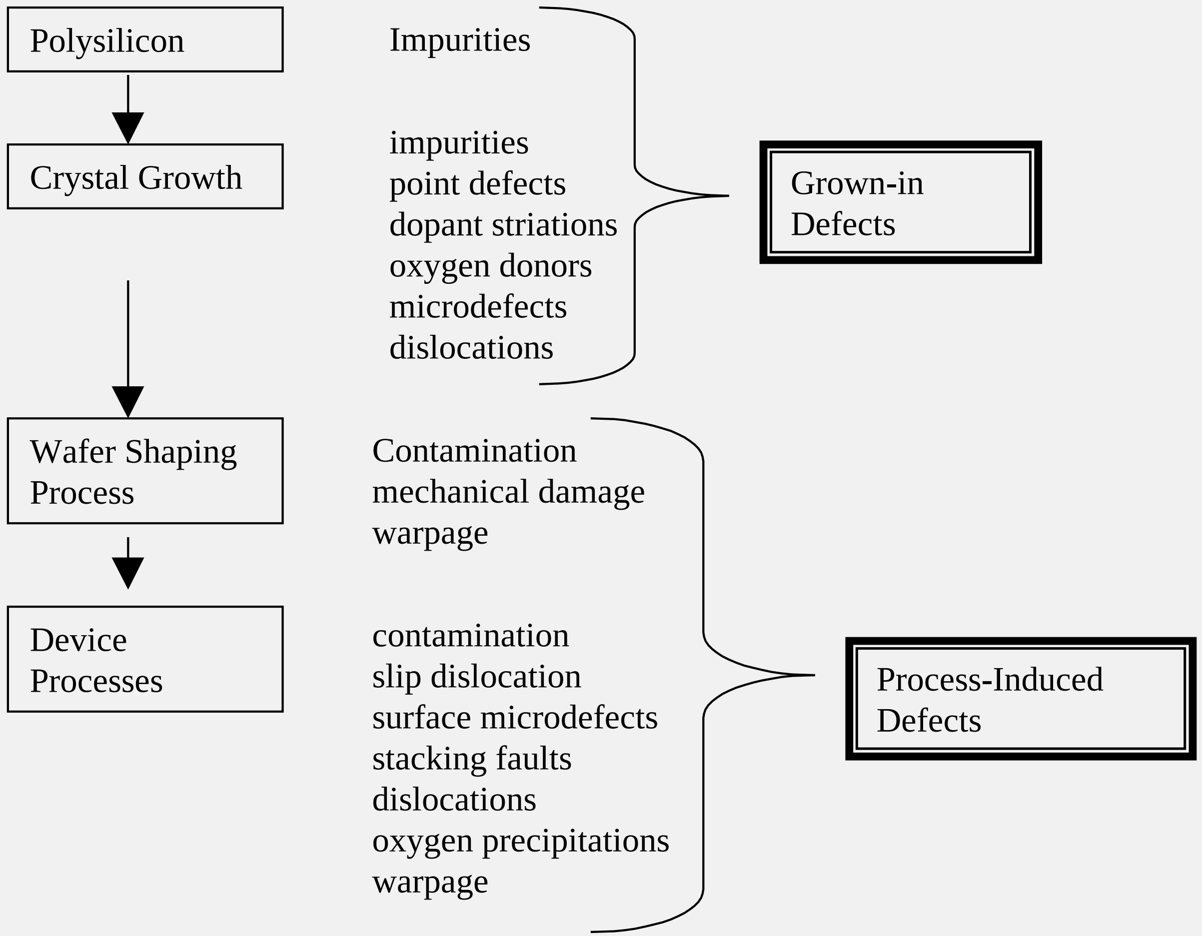


Forecast of Si wafer production 2005



BSI – billion square inches

Defect generation



Point defects and jewelry

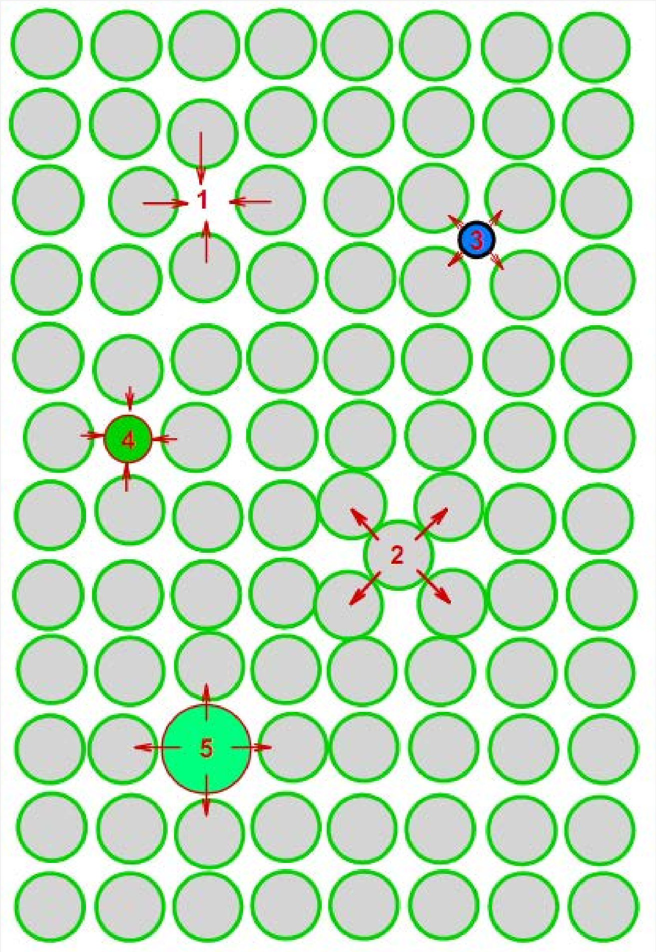
(1) vacancy

(2) self-interstitial

(3) interstitial impurity

(4),(5) substitutional impurities

arrows – local stresses

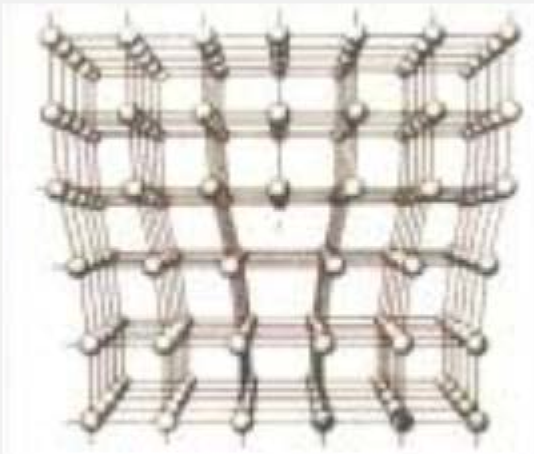


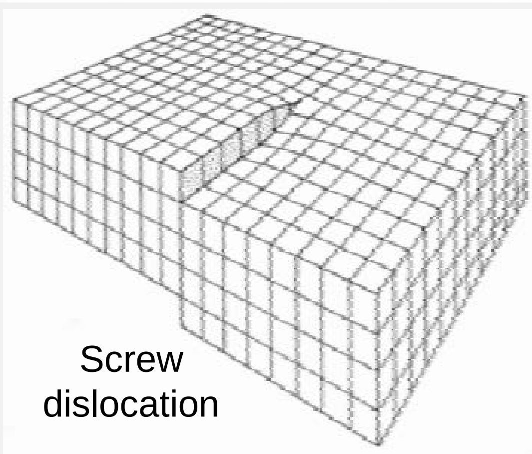
Ruby – Cr in Al_2O_3 matrix

Sapphire – Ti and Fe in Al_2O_3

Line defects (dislocations) and damascus steel

Edge dislocation





Summary I

- Silicon posses unique set of functional properties
- Silicon is easily processed during fabrication
- Si forms thermal oxide with excellent functional properties and it can be used as mask
- Si is cheap and abundant on the Earth

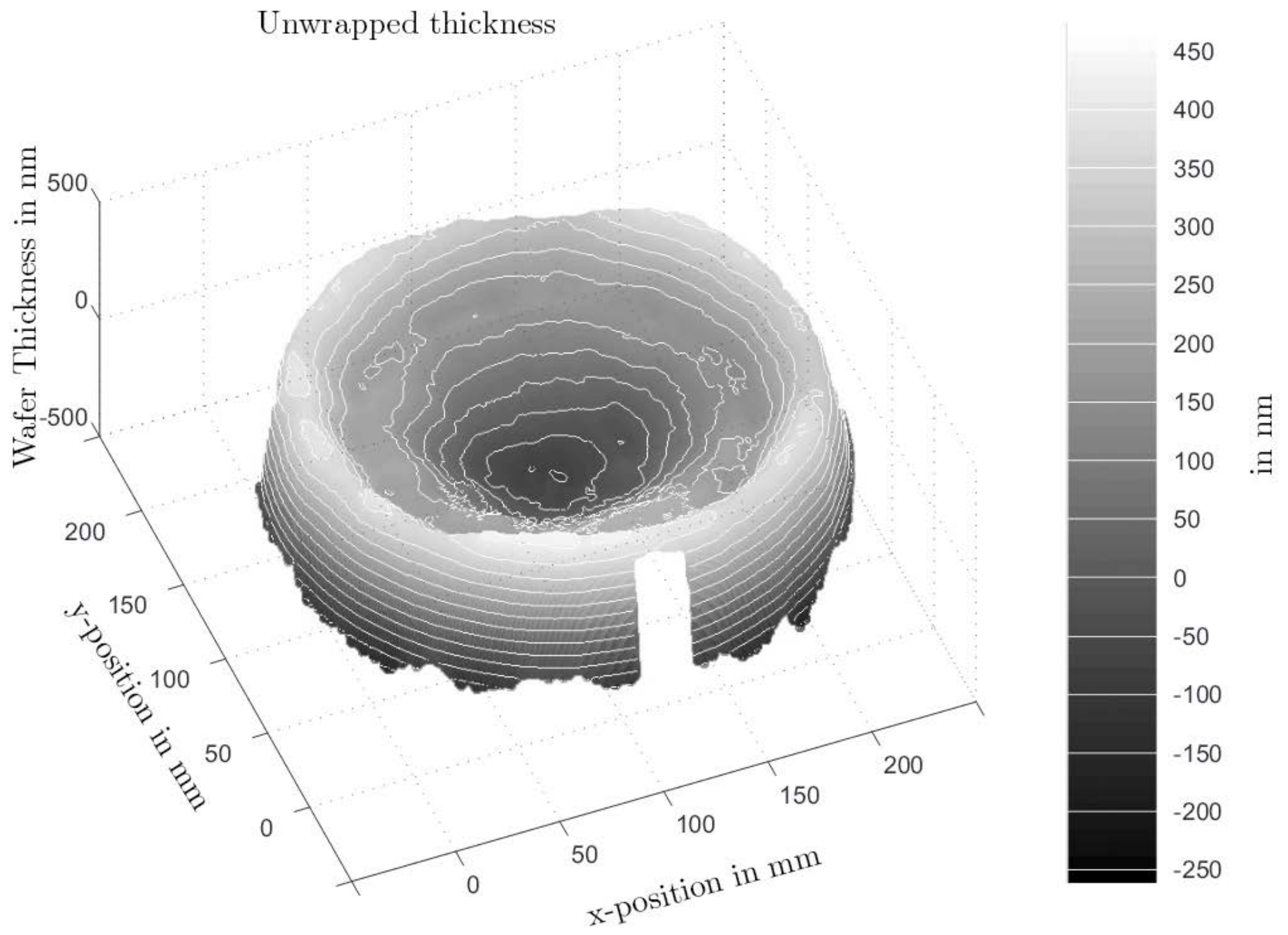
-> as a result

- The best ratio ”function to price”

Advanced wafers (substrates)

- Functions: mechanical support, providing functional properties (electronic, optical etc.)
- Circular wafer
  - Si, GaAs, SiC, Ge, quartz, glass
- Square plate
  - glass, polysilicon, ceramics
- Film, foil
  - polymers: polyimide, PDMS, kapton
  - metals: Al, Cu

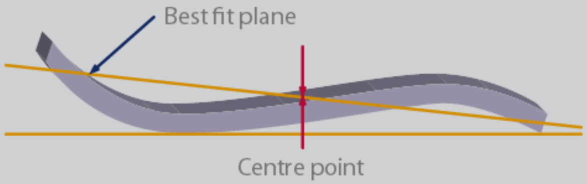
Wafer thickness measurements

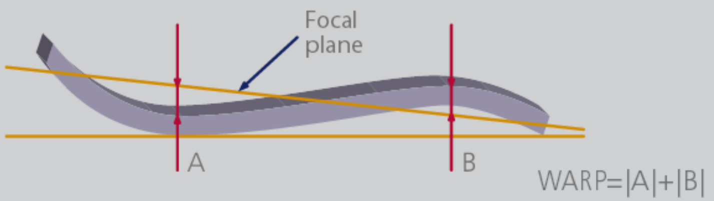


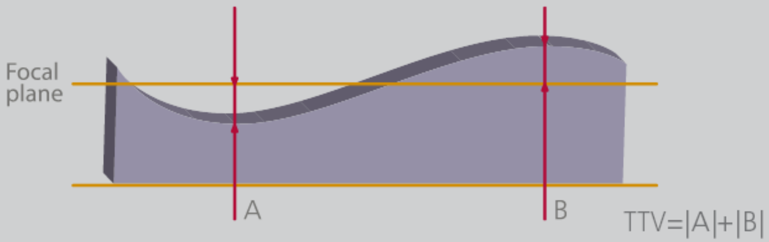
Maarten J. Jansen, HanHaitjema, Peter H.J. Schellekens
Eindhoven University of Technology, Precision Engineering Section, Eindhoven, The Netherlands

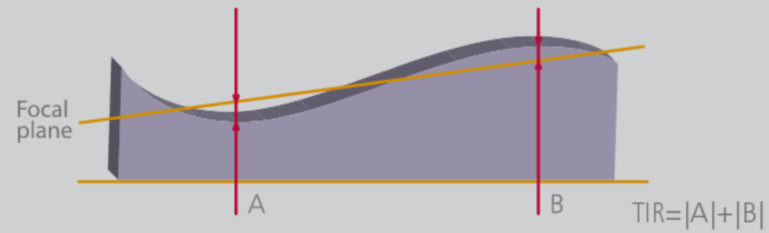
Global flatness specifications

Bow	Distance between the surface and the best fit plane at the center of an unclamped wafer.
Warp	Sum of the maximum positive and negative deviations from the best fit plane (wafer unclamped).
TTV Total Thickness Variation	Difference between the maximum and minimum values of the wafer thickness (wafer clamped).
TIR Total Indicated Reading	Sum of the maximum positive and negative deviations from the best fit plane (wafer clamped).



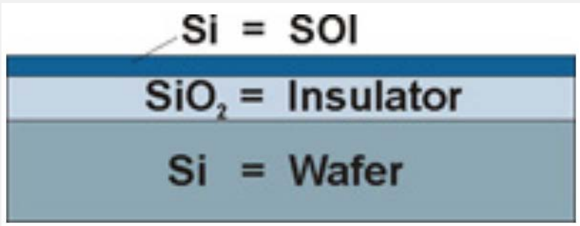






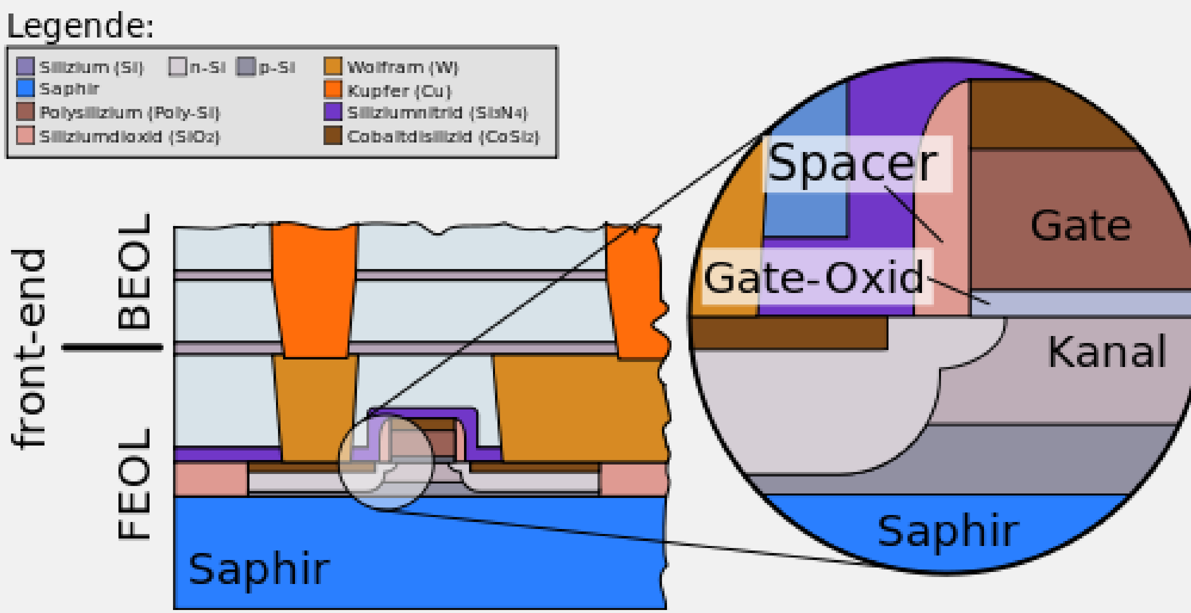
SOI and SOS wafers

Silicon on isolator (SOI)



Simplify chip fabrication, but wafers are very expenssive!

Silicon on sapphire (SOS)



Unusual substrates

Mobility enhancement

Thermal management

System-on-chip

Memory solutions

Table 1. Emerging materials status*

Emerging material	First year coverage	Chip products on market	Close to mainstream acceptance	Change of importance since 2005		
				Increased	No change	Decreased
Global strained Si	2003	No	No		•	
Global strained SOI	2003	No	No	•		
Germanium channel transistors	2003	No	No	•		
III-V channel transistors	2007	No	No		N/A	
Isotopically pure Si	2003	No	No			•
Silicon on diamond	2005	No	No		•	
Silicon on SiC	2005	No	No		•	
Silicon on alumina	2005	No	No		•	
Channel orientation	2005	Yes	Yes	•		
Surface orientation	2005	No	No		•	
Carbon nanotubes	2005	No	No		•	
High resistivity Si	2003	Yes	Yes	•		
Optical interconnection on Si	2003	No	No		•	
Phase change memory	2007	No	No		N/A	

*listing the technologies that have been covered by the *ITRS* Emerging Materials committee since its inception in 2003, along with several status columns.

Summary II

- Wafers can be distinguished by:
  - material
  - doping
  - crystal orientation
  - shape
  - size
  - polished sides
  - grown layers