On the Way to Zero Defect of Plastic-Encapsulated Electronic Power Devices—Part III: Chip Coating, Passivation, and Design

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***Abstract*—Concerning thermomechanically induced failures such as metal-line deformation and passivation cracks, there is a practicable way to achieve the zero-defect limit of plastic-encapsulated power devices. This limit can be reached by, first, evaluating the influence of the major components involved and, consequently, by selecting the appropriate materials and measures, and, second, by always keping in mind the interdependence between all components, i.e., chip and package have to be regarded as an entity. An important finding was that applying simply one improvement step will not necessarily lead to the desired goal. Only the implementation of all improvement steps considering their interdependence is the key for the perfect overall system chip and package. In Part III of this series of papers, the influence of passivation and die coating materials on thermomechanical damage is investigated. Finally, it is shown that an intelligent chip design, in combination with a stiff Al multilayer, a low-stress molding compound (low coefficient of thermal expansion and high Young's modulus), a new passivation material, and an appropriate polyimide layer, may reduce the thermomechanical damage to zero, even for electronic power devices.**

***Index Terms*—Design, finite-element-method (FEM) simulation, passivation, passivation cracks, polyimide (PI), power device, thermomechanical stress, zero defect.**

I. Introduction

PLASTIC encapsulation of semiconductor integrated circuits (ICs) always induces mechanical stress within the devices. The resulting defects like metal-line deformations and cracks in brittle passivation are still a major reliability concern. The root cause is the difference between the coefficient of thermal expansion (CTE) of molding compound (MC) and silicon (Si), which leads to a thermomechanically induced shear stress. These cracks can propagate into the insulating dielectric layers to the lower metal lines, causing electric shorts by means of protruded metal, as well as electric opens or leakage currents, if moisture penetrates the MC from the outside and corrosion occurs. Examples have been shown in Parts I and II of this series of papers [1], [2].

To minimize this failure root cause requires one to optimize the statics of the Overall system Chip and Package (OCP), as well as the deformation behavior of the involved components. To prevent the passivation cracks, some lessons were already learned in the past [3]–[12]. One of the most important, for instance, was the demand for good adhesion [13] between all parts of a device (OCP). Thus, the device interfaces have all been optimized as far as adhesion was concerned. While coating the chip with polyimide (PI) [14]–[16] has strengthened the MC/chip interface, adhesion between MC and lead frame has been improved by applying a special treatment [17]. The passivation layer was introduced in the 1970s as an indispensable protection coating of Al metal lines against corrosion [3]. It was found that thicker layers are more stable concerning cracking [7]. Furthermore, the impact of chip design [18]–[23] has been analyzed in more detail. As a result, the advantage of slotted broad metal lines in the corner and edge regions, as well as of 45° inclined lines in the corner region, has been recognized. In spite of these precautions, in the case of power ICs, however, a considerable number of passivation cracks still occurred after temperature cycling.

The aim of this series of papers is to demonstrate that there is a practicable way to reach the zero-defect frontier after temperature cycling stress by, first, evaluating in detail the influence of the major components involved and, consequently, by selecting the appropriate materials and measures, and, second, by always keeping in mind that chip and package have to be regarded as an entity (OCP).

In Part I of this series of papers [1], it was shown that the yield stress of power metallization plays a crucial role for the failure mechanisms of passivation cracking and metal-line deformation, as generated during temperature cycling stress. The introduction of a material with a distinctly increased yield stress was the first big step on the way to zero defect. This was achieved by the introduction of the Al multilayer. Furthermore, it was shown that at least four Al layers separated by 20-nm TiN (4× multilayer) were necessary to reduce the number of passivation cracks and the metal deformation distinctly.

In Part II, the influence of the MC and its governing parameters CTE and Young's modulus was investigated, and the criteria for the best choice of an MC were elaborated. A simple closed-form linear elastic theory [24] was applied to get a first "rough" ranking of MCs. For MCs with different CTEs, the result was clear: The smaller the CTE, the smaller the generated damage. Finally, the possibility of a fine ranking of MCs with constant CTEs but different Young's moduli was demonstrated by finite-element-method (FEM) simulations under consideration of the viscoelastic behavior of the materials. As a result,

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the MC with a higher Young's modulus was found to produce less damage.

In this paper (Part III), the impacts of chip coating (PI) and passivation material are studied in Sections II and III, respectively. In Section IV, the role of chip design is discussed, and a design optimization, as performed by FEM simulation, is proposed. Finally, discussion of the results and conclusions are presented in Section V.

The test vehicle used in the next sections was a P-DSO36 device molded with MC A ($\mathrm{CTE}_1 = 14 \cdot 10^{-6}$ K^{-1} and $E_1 =$ 15.1 GPa) and MC D ($\mathrm{CTE}_1 = 6.1 \cdot 10^{-6}$ K^{-1} and $E_1 =$ 34.7 GPa). Both MCs were characterized viscoelastically in [2, Section IV, Part II]. The chip size was $7.3 \times 4.1 \times 0.38$ mm^3 (chip C1; see [2, Section III, Part II]).

II. Chip Coating

There are two ways to reduce the internal stress at the chip surface: to use a low-stress MC and to introduce a buffer layer against stress. The best results are obtained by using both simultaneously. In our case, the buffer material between silicon die and MC is a PI layer [14]–[16]. The function of this layer is twofold. On the one hand, the adhesion between passivation and MC is improved, while on the other hand, a plastic relaxation is expected, i.e., the PI acts as a buffer against shear stress. Consequently, parameters such as adhesion, as well as elongation to yield and elongation to break, have to be considered. The behavior of the PI after temperature cycling stress is used to assess its performance. Fig. 1 shows an example of an inappropriate PI material after 1000 TC. The layer is strained and therefore oriented on a molecular level [see Fig. 1(a)] and cracked after the elongation to break has been exceeded [see Fig. 1(b) and (c)].

The buffer effect of the PI layer should increase with its thickness [15], [16]. This has been verified by FEM simulations (see Figs. 2 and 3). As a result, the shear stress acting at the passivation topside near the chip edge decreases by about 25% when the PI thickness is increased from 6 to 21 μm.

This shear stress reduction should directly affect the deformation (wrinkling) of the power metal layer. The influence of an increasing PI layer thickness on the thermomechanically induced damage has been investigated experimentally with MC A. Fig. 4 shows the results after 1000 TC. The metal deformation reduces distinctly when the PI layer thickness is increased from 6 to 21 μm.

As shown previously, a PI material with a sufficient elongation to break and a sufficient layer thickness must be taken into consideration. Concerning the CTE and Young's modulus, it is not obvious which material is the appropriate one. Consequently, two PI materials have been characterized: material X with $\mathrm{CTE} = 45.7 \cdot 10^{-6}$/K and $E = 1.98$ GPa, as well as material Y with $\mathrm{CTE} = 39.5 \cdot 10^{-6}$/K and $E = 2.37$ GPa. The values for the Young's modulus E given here have been determined at -40 °C and an elongation of 3%. The whole stress–strain curves (see Fig. 5) have been measured by means of DMA in tensile mode. The dimensions of the samples were $30 \times 10 \times 0.02$ mm^3.

The experimental results show that up to 240 °C the elongation to break of material Y is distinctly higher than the one of material X. This correlates with the finding that, after 1000 TC, material X had internal cracks (see Fig. 1) while material Y remained intact.

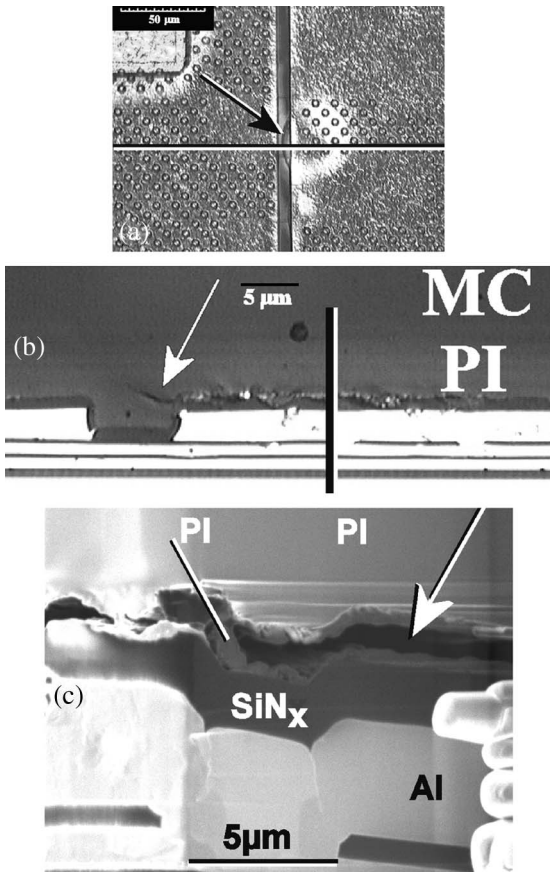

Fig. 1. Cracked PI layer after 1000 TC (material X, see in the following). (a) Overview of a mechanically stressed PI region and a crack front (arrow, polarization microscopy of the die topside after removing the MC). The line shows the position of the cross section in (b). (b) Cross section through the stressed PI area shown in (a). (Arrow) The PI coating is cracked. The vertical line shows the position of the FIB section in (c). (c) FIB section showing that the crack propagates through (arrow) the PI layer. The adhesion between passivation and PI is not affected.

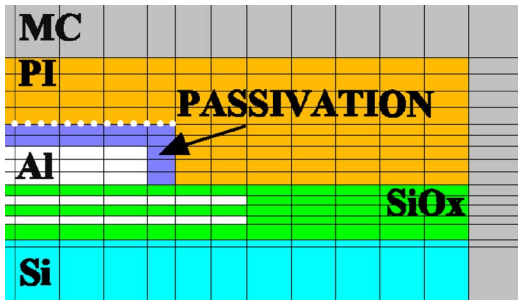

Fig. 2. Detailed view of the right-hand edge of the 2-D model used for the package P-DSO36. The white dotted line indicates the position where the shear stress τ was calculated by FEM simulation.

Finally, the metal shift during TC has been simulated by FEM, as described in [2, Section IV.B, Part II]. In the case of the PI layer, a nonlinear elastic approach for the material model was used by implementation of the material properties deduced from Fig. 5. As can be seen in Fig. 6, there is no distinct difference between the two materials. Nevertheless, a similar

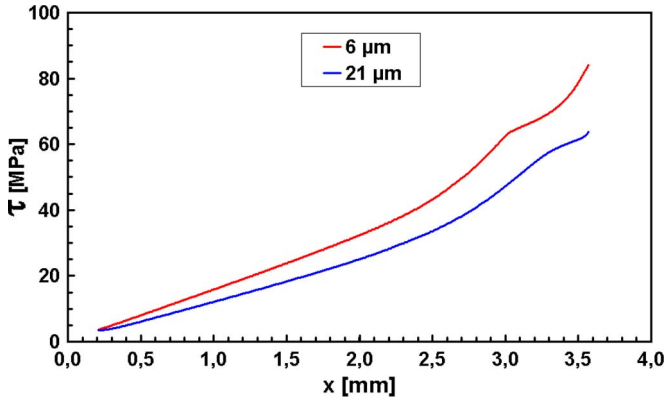

Fig. 3. Shear stress τ over the passivation layer covering an Al plate as a function of the distance from the die center $\mathbf{x}$ for 6- and 21-μm-thick PI coatings (material Y, see in the following; the MC was of type A).

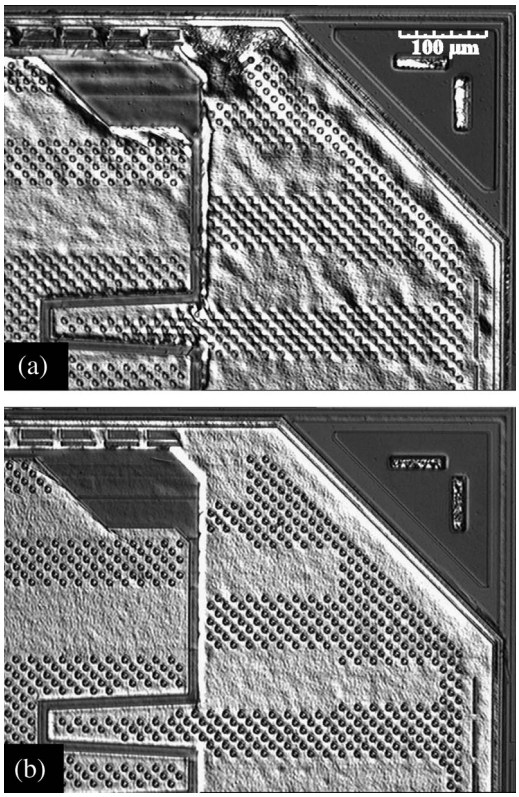

Fig. 4. Wrinkling of a 3.5-μm 4× Al multilayer in a chip corner after 1000 TC, as induced by MC A. The PI coating layers (material Y, see in the following; the MC was of type A) were (a) 6 μm thick and (b) 21 μm thick (Nomarski interference contrast microscopy).

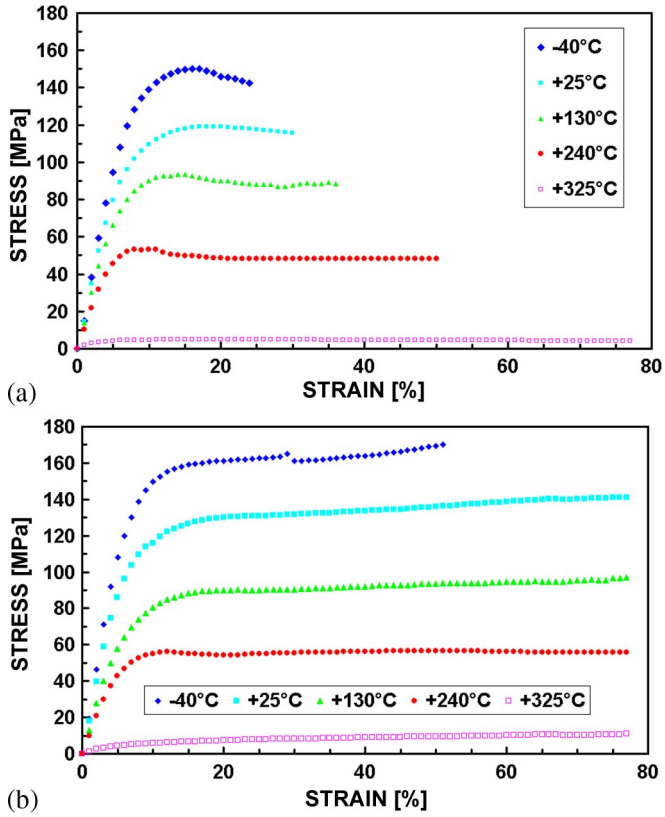

Fig. 5. Stress/strain curves for (a) PI X and (b) PI Y at various temperatures.

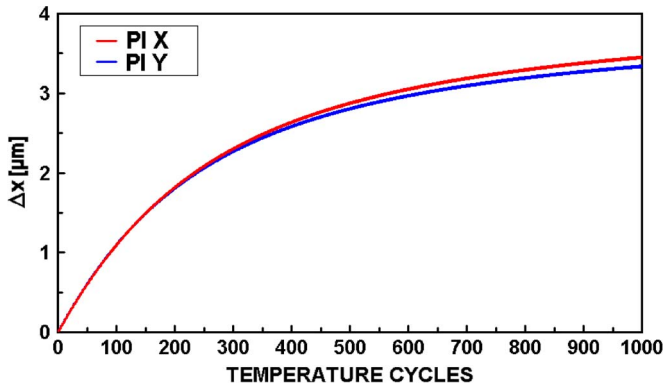

Fig. 6. FEM simulations of the metal shift Δx during temperature cycling stress (see [2, Part II, Fig. 13 (arrow 2)]) for PI X and PI Y, respectively. The same cycling conditions, as shown in [2, Part II, Fig. 14], were used. The MC was of type D.

trend as in the case of the MC can be observed (see [2, Part II]): Material Y with small CTE and large Young's modulus E leads to a smaller metal shift than material X with large CTE and small E.

The investigation of passivation cracks after 1000 TC revealed that using PI material Y with a layer thickness of 21 μm leads to a further damage reduction. Unfortunately, it turned out that too thick PI layers have some adverse effects concerning, e.g., wafer bow and wire bonding process. As a compromise, a layer thickness of 16 μm has been selected. Thus, passivation cracks are not yet totally prevented. Passivation material and chip design have to be addressed in addition.

III. Passivation Material

The passivation layer as an indispensable coating of IC metal lines against corrosion has been introduced in the mid-1970s [3]. The main reason was the change of the packaging technology from metal and ceramic to plastic-based packages. Optimizing the mechanical properties of passivation and interlayer dielectrics requires a parameter that measures its resistance against cracking under mechanical stress. A straightforward choice may be the fracture toughness K_{1c}, which is a measure for the material's stability against punctual mechanical stress. K_{1c} is determined usually by means of microindentation and/or nanoindentation [25]. Hereby, only indentation depths

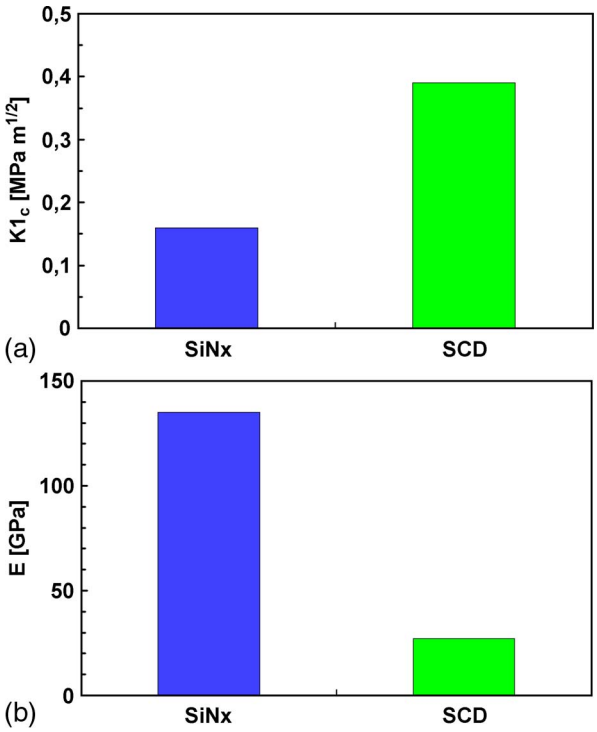

Fig. 7. Comparison of the standard SiN_x and the SCD material. (a) K_{1c}. (b) Young's modulus.

that are distinctly smaller than the layer thickness must be considered.

In this evaluation, a plasma nitride passivation consisting of 1-μm SiN_x and 0.3-μm SiO_2 underlayer was compared with a newly developed silicon–carbon-based-dielectric (SCD) material of the same thickness and underlayer. Both sandwiches were deposited on a 3.5-μm Al layer. The fracture toughness of this new material was higher by more than a factor of two in comparison to the SiN_x standard passivation [see Fig. 7(a)].

In addition, the Young's modulus of the SCD, as determined also by nanoindentation and by bulge measurements, is significantly lower than the corresponding value of the standard passivation [see Fig. 7(b)].

Based on these properties, the SCD is expected to be superior concerning its robustness against crack formation. This was confirmed by TC experiments. As shown in Fig. 8, the amount of passivation cracks was distinctly reduced in the case of the new SCD material.

Other than the low Young's modulus, the SCD material turned out to undergo large deformations without reaching the fracture limit. This was observed from focused-ion-beam (FIB) cuts through the tilted edges of broad aluminium plates covered with the passivation layers under evaluation. After 1000 TC, the standard passivation showed the well-known cracks at critical positions [see the arrows in Fig. 9(a)], while in the case of the new passivation material, distinctly less cracks appeared at these positions [see Fig. 9(b)].

As a conclusion, the new SCD material led to a further distinct quality improvement of the power ICs. However, the zero-defect limit was still not reached. One important and promising optimization possibility still exists, namely, the chip design. This will be discussed hereinafter.

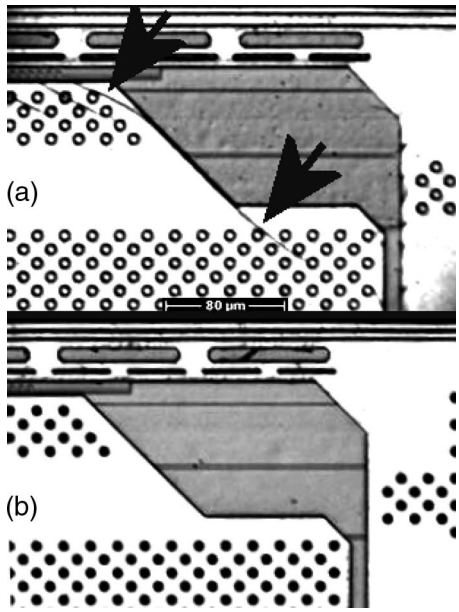

Fig. 8. Typical passivation cracks in a chip corner after 1000 TC in the case of the (a) standard SiN_x passivation and the (b) new SCD material, where no cracks occurred. The power metallization was an Al 4× multilayer, the PI thickness was 16 μm (type Y), and the MC was of type D. The passivation layer thickness in both cases was 0.8 μm, and the SiO_2 layer underneath was 0.3 μm thick.

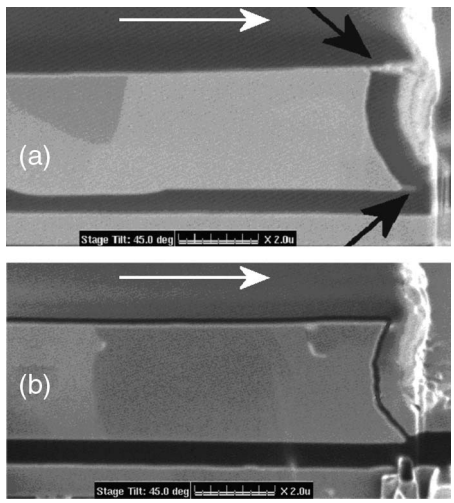

Fig. 9. (Black arrows) Typical cracks after 1000 TC at the edge of a shifted aluminium plate for (a) standard SiN_x passivation and the (b) corresponding situation in the case of the SCD material (FIB sections). The power metallization was a 3.5-μm single Al layer, the PI thickness was 16 μm (type Y), and the MC was of type D. (White arrows) The shearing force was acting from left to right.

IV. Design

In [1, Part I], [2, Part II], and Sections II and III of this paper (Part III), the mechanical properties of the materials used in semiconductor devices have been treated, and their evaluation has been shown. Exposing the devices to thermomechanical stress leads to their degradation. One characteristic of this degradation is the cracking of the passivation layer, which was analyzed here in more detail.

As discussed in the technical literature [18]–[23], a possibility to improve the stress situation within the passivation

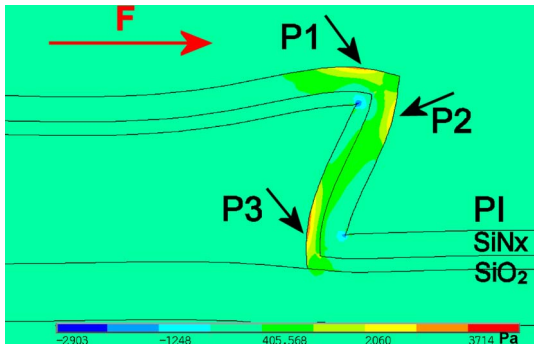

Fig. 10. Principal stress S1 at −55 °C after 1 TC, as obtained from a 2-D simulation (F is the thermomechanical shear force). The positions of the three areas of high principal stress S1 are denoted by P1–P3 (the deformation is shown disproportionately).

layer is given by reducing the width of metal lines. One can realize this by slotting broad lines and plates in the edge and corner regions. The efficiency of this method was impressively confirmed in the past with simple test chips consisting basically of one passivated metal layer [18], [23].

Based on the material data evaluated in [1, Part I], [2, Part II], and Sections II and III of this paper (Part III), a realistic simulation of the mechanical stress in the passivation layer became possible. In a first step, a 2-D simulation of the situation in the edge region of a metal line was performed using the submodeling technique [26]. Thus, a precise view into the states of strain and stress for this typical cross section was obtained. The results of this simulation are shown in Fig. 10. Because of the model's complexity, only one temperature cycle was calculated. The simulated 2-D cross section lies parallel to the direction of the thermomechanical shear force F. Three areas with very high principal stress S1 could be identified; their positions are denoted by P1, P2, and P3.

In order to understand the influence of the design on the states of strain and stress, a 3-D simulation is, however, required. Thus, in a second step, 3-D simulations of different design versions were evaluated. One example is shown in Fig. 11 (for details concerning the 3-D submodeling technique, see also [26]). Again, because of the complexity of the 3-D model, only one temperature cycle was simulated. The positions of the stress peaks detected here correspond well to the positions found in the 2-D simulation discussed earlier. These stress regions have been analyzed by means of SEM. A very good agreement between the predicted regions of maximum stress and the crack locations was observed (see Fig. 11).

This ability to predict the starting points of the passivation cracks made it possible to compare different design alternatives. As a result, recommendations for a robust design could be deduced. For instance, the maximum stress at position P1 (see Fig. 10) has been reduced by about 25% using a design that avoids large power metal plates in the corner and edge regions (see Fig. 12).

An additional outcome of the FEM simulation was the evaluation of the influence of the chip size (area) and chip aspect ratio. For a given area, the minimum stress is reached in the case of a quadratic chip (aspect ratio = 1).

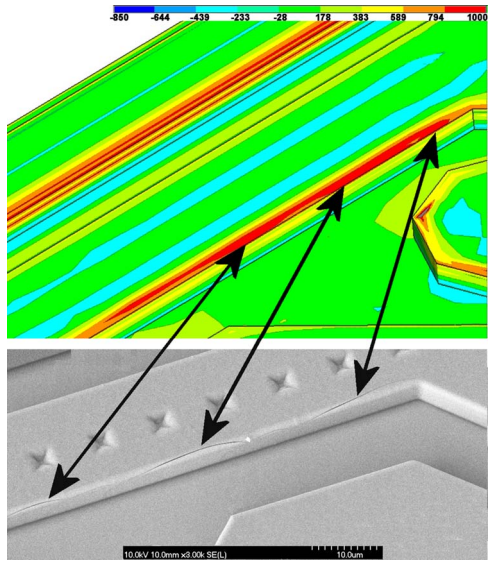

Fig. 11. Principal stress S1 in the passivation layer at −55 °C after one temperature cycle, as obtained from a (top image) 3-D simulation. The top-right corner of the chip is shown. (Arrows) The positions of the stress peaks correspond well to the (bottom image) locations of the cracks observed after 1000 TC by SEM. The power metal was a 4× Al multilayer covered by 16-μm PI (type Y); the MC was of type D.

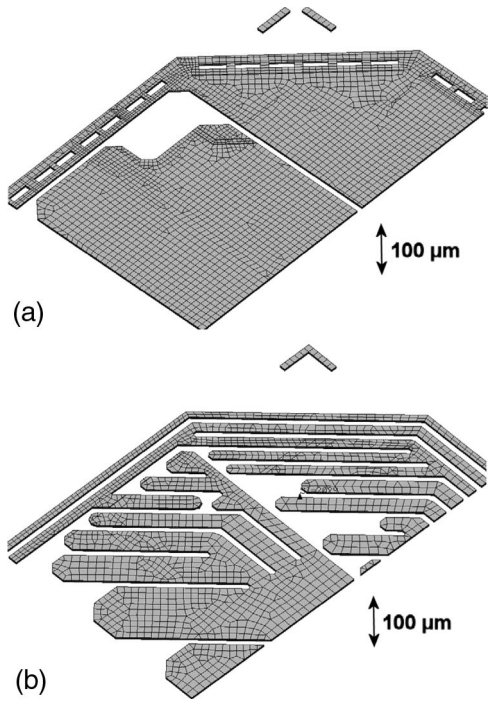

Fig. 12. Comparison of (a) conventional and (b) optimized designs of the passivated power metal layer in the top-right corner of the chip.

V. Discussion and Conclusion

It has been shown in [1, Part I], [2, Part II], and the sections of this paper (Part III) that the ambitious goal to reach the zero-defect frontier is achievable, even in the case of electronic power devices. First, the influence of the major components involved in the construction of an electronic power device must be evaluated in detail. As a consequence, the appropriate materials have to be selected, and additional measures must

be taken for a robust device (e.g., design). Second, it must always be kept in mind that chip and package have to be regarded as an entity (OCP). A summary of the steps taken and lessons learned on the whole way to zero defect is given in the following.

1) The power metallization was shown to play a crucial role for the failure mechanisms of metal deformation and passivation cracking. Understanding the ratcheting mechanism led to the introduction of a layered Al/TiN metallization with a distinctly increased yield stress. The development of such a metallization was accompanied on the one hand with microcompression experiments and passivation crack monitoring, as well as with FEM simulations on the other hand.
2) The thermomechanical influence of the surrounding MC on the chip, i.e., the root cause of the passivation cracks, was studied in detail. A simple closed-form linear elastic model of a three-layered structure showed the CTE to play a key role concerning metal deformation and passivation cracking and allowed a "rough" ranking of various MCs: The smaller the CTE, the smaller the damage. The Young's modulus turned out to influence cracking in an unexpected manner: For MCs with the same CTE, the number of cracks decreases with an increase of Young's modulus. A correct FEM simulation of this effect was possible only after taking into account the viscoelastic properties of the MCs.
3) The thermomechanical influence of the MC was reduced by introducing a PI layer. The function of this layer is twofold. On the one hand, the adhesion between passivation and MC is improved, while on the other hand, the PI acts as a buffer against shear stress. Experiments, as well as FEM simulations, revealed that PIs with small CTEs and thicker layers reduce the damage and the shear stress in the passivation.
4) A new silicon–carbon dielectric material was developed, and its superiority to former materials was demonstrated by nanoindentation tests and confirmed impressively by passivation crack evaluation.
5) The influence of the power metal design on the amount of passivation cracks was investigated in great detail. A 2-D simulation of a typical metal-line cross section revealed the points of highest principal stress after 1 TC. Corresponding 3-D simulations showed that, even after one temperature cycle, the positions of the stress peaks correspond very well not only to those found in the 2-D case but also to the crack locations observed by SEM investigations. Thus, the 3-D simulation now enables one to forecast even the sites of cracks observed after temperature cycling. As a result, a robust design could be deduced, which led to a distinct reduction of the principal stress at the most critical positions and, consequently, to a reduction of passivation damage.

The way to zero defect is shown in Fig. 13: the starting point was more than 1000 cracks per sample for the case of standard materials and design. Metallization and MC improvement reduced passivation damage drastically and allowed now to use the number of cracks as a quantitative measure of this damage (Al multilayer and MC D instead of single layer and MC A; see [1] and [2]). Using the appropriate PI (type Y) and passivation material (SCD) and optimizing the chip design finally resulted in about one crack per device. This crack occurred at the edge of the bond-pad opening window, i.e., at a totally uncritical position without any relevance for the reliability.

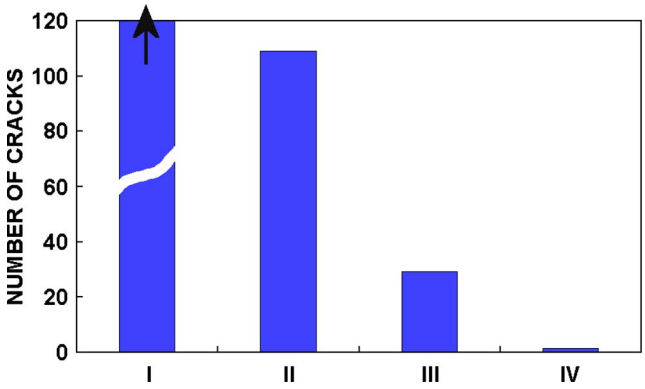

Fig. 13. Reduction of crack numbers after various improvement steps. (I) Old materials and design (Al-single layer/MC A/6-μm PI/passivation SiN_x/old design). (II) Al multilayer/MC D/16-μm PI/passivation SiN_x/old design. (III) Al multilayer/MC D/16-μm PI/passivation SiN_x/new design. (IV) Al multilayer/MC D/16-μm PI/passivation SCD/new design.

From Fig. 13, it can also be derived that applying simply one improvement step will not lead to the desired goal of zero defect. The reason is the strong interaction between all components within an electronic power design (OCP). Consequently, the implementation of all improvement steps with their interdependence is the key for the perfect OCP.

All results discussed here were obtained with a package having a relatively thick MC overchip layer (about 1.6 mm). According to FEM simulations and other technical literature [23], it can be regarded as a matter of fact that, in the case of thinner packages, the number of cracks will be reduced to zero.

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