Process integration

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Chapter 25

Previous material

- Bonding
- CMP
- CMOS

Outlook

- Wafer selection
- Metal-semiconductor contact
- Thermal budget
- Pattern limitations
- Design rules

From process steps to functional device

Input wafer

Masks

Thin film formation

Doping

Lithography

Etching

Output wafer

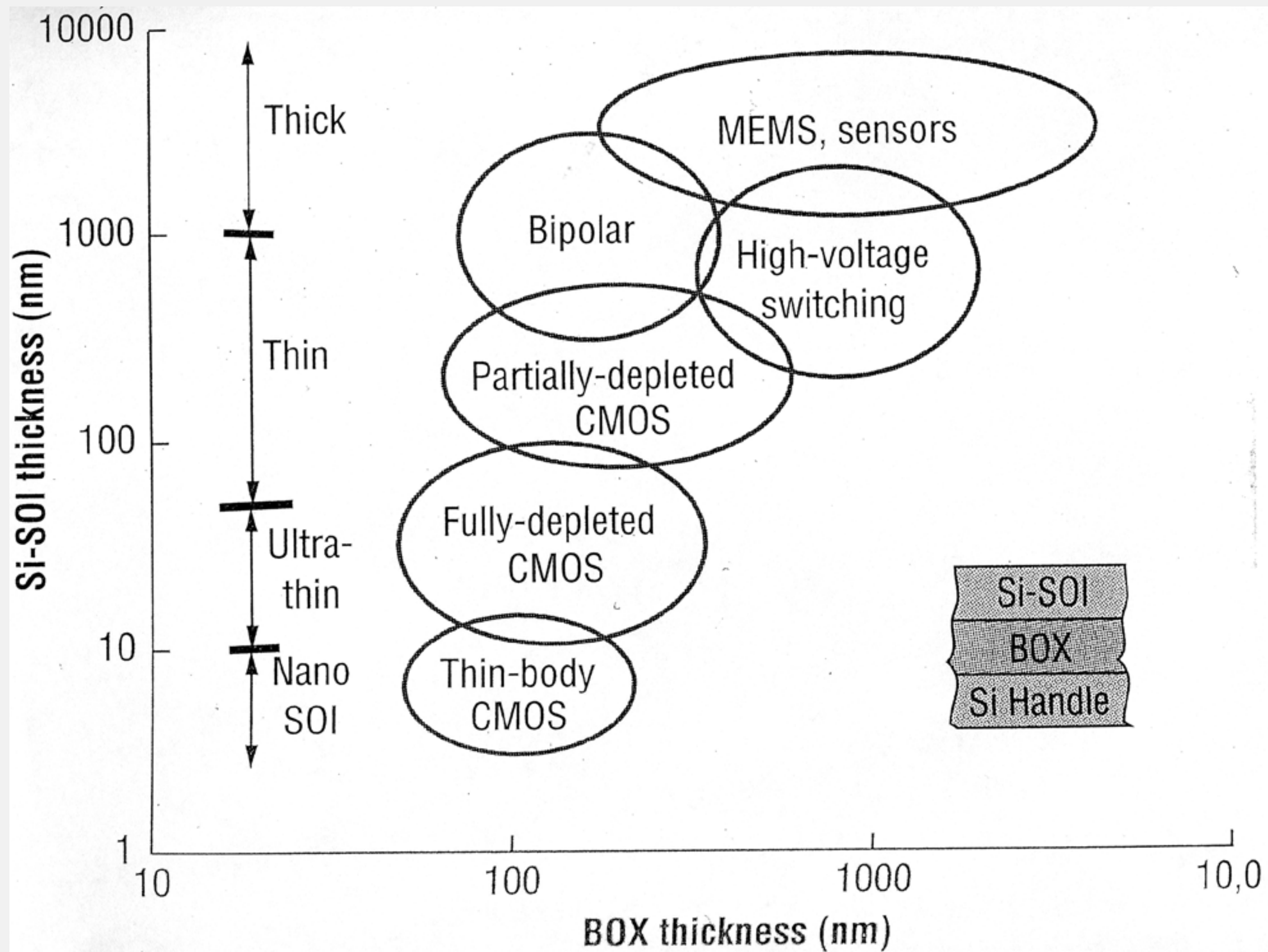
Process integration components

- Wafer selection:
- n-type or p-type, epitaxial or SOI wafers, resistivity, TTV
- Materials compatibility:
- Interfaces, thermal stresses, chemical properties
- Process and device parameters:
- Variation of diffusion profiles, etch profiles, lithographic linewidth…
- Design rules:
- CD, alignment rules
- Mask considerations:
- Critical and non-critical masks, undercut compensation, test chips
- Order of process steps:
- Annealing effect, released structures, frontside vs. backside
- Reliability:
- current densities, stresses, breakdown voltage

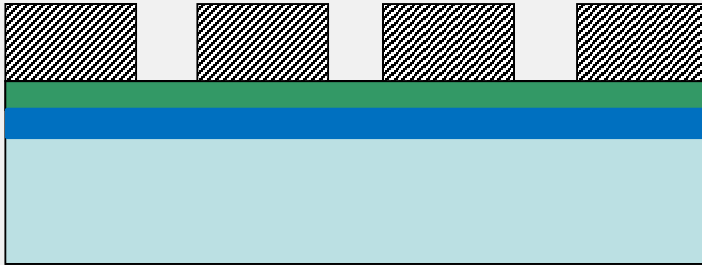
Wafer selection

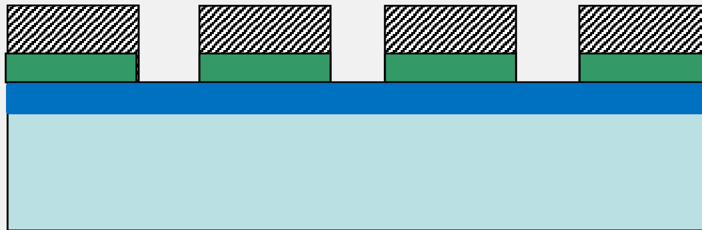
- active role for the wafer (electronic properties)?
- passive role ?
  - thermal conductivity
  - optical transparency
  - flat, smooth, mechanical support
- compatibility with equipment ?
- thermal limitations ?
- contamination ? Especially glass in Si fabs !

SOI wafers: layer thicknesses



Metal heater processing

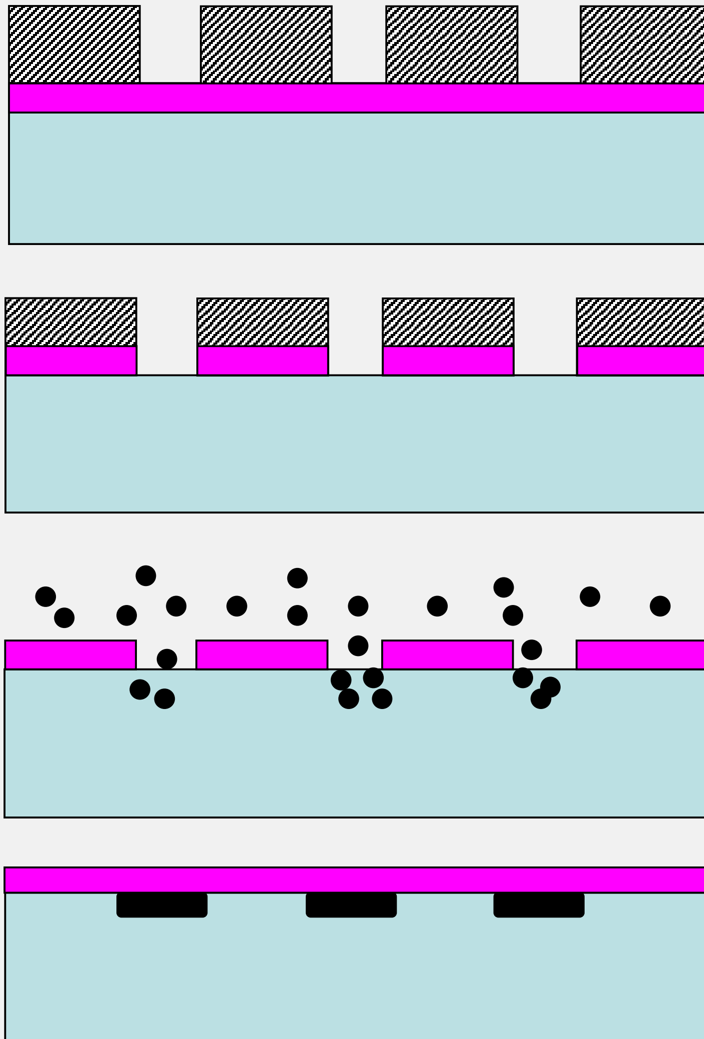




1. Silicon wafer, no specific specs
2. Insulator deposition
3. Metal sputtering (or evaporation)
4. Lithography with resistor mask

5. Metal etching & resist stripping

Diffused heater processing

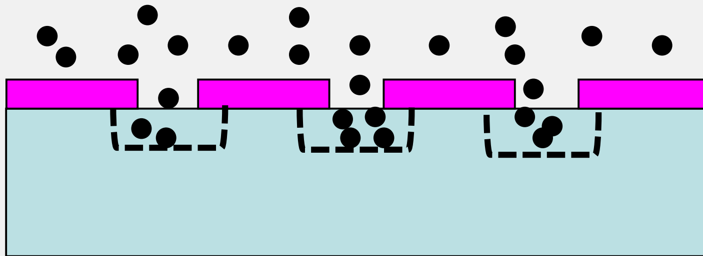


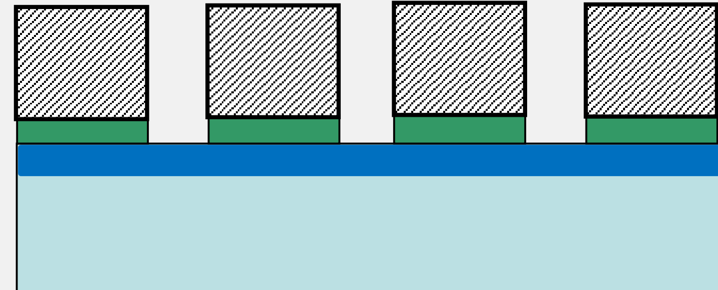
1. ***Cleaning***
2. Thermal oxidation
3. Lithography with heater mask
4. Oxide etching + resist strip
5. ***Cleaning***
6. Diffusion (in furnace)
7. Oxide etching + resist strip
8. ***Cleaning***
9. New thermal oxidation !

Diffused vs. metal resistor

Heats up substrate
Ohmic contact is a problem

Heats up films below and above
Ohmic contact is easy done





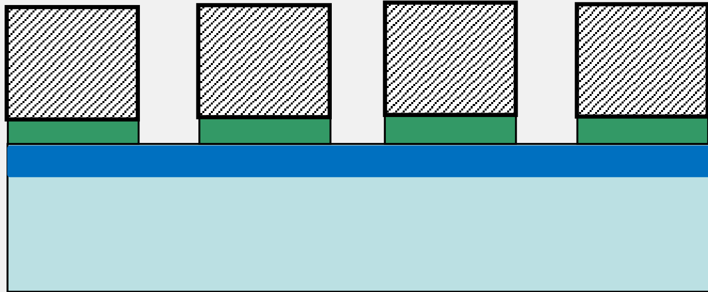
Size determined by:
Lithography + diffusion
Always isotropic !!

2 µm linewidth +
1 µm diffusion depth ➔
1 µm sideways diffusion
➔ 4 µm wide resistor

Size determined by:
Lithography + etching
Can be anisotropic.

2 µm linewidth ➔
2 µm wide resistor

3rd option: polysilicon resistor



1. Silicon wafer
2. Oxide (insulation)
3. Poly deposition (CVD)
4. Poly doping
5. Lithography
6. Poly etching + strip PR

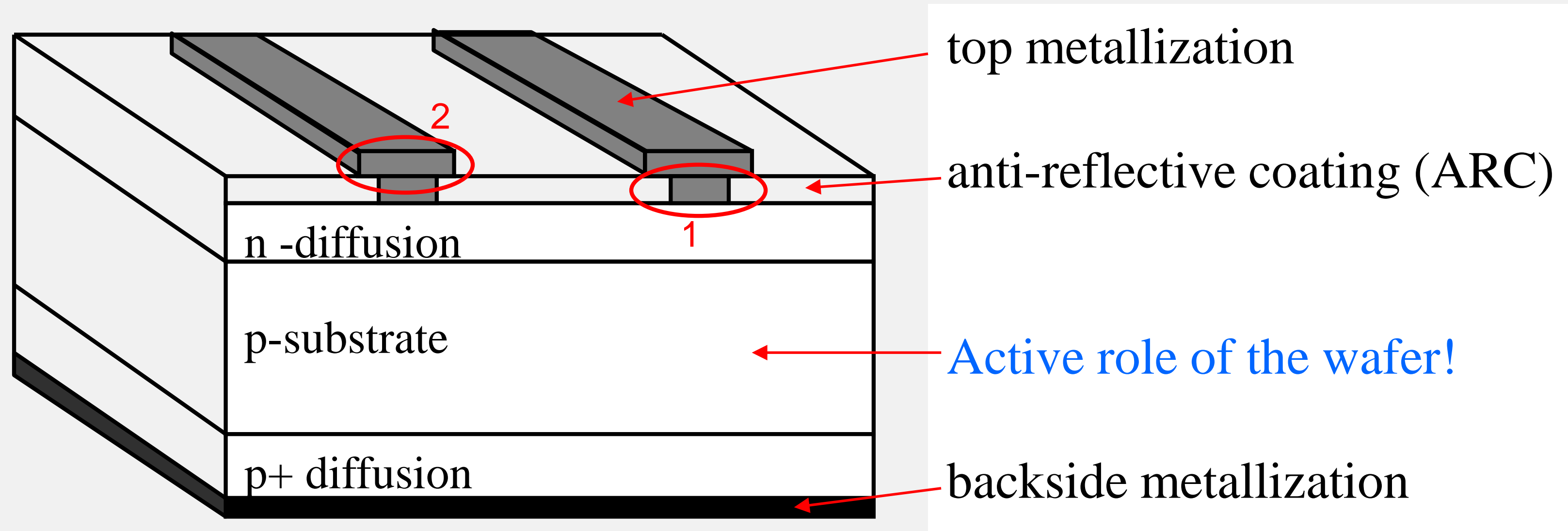
Why is poly resistor option useful ?

Polysilicon resistivity can be tailored over a vast range.

Polysilicon can be thermally oxidized.

Polysilicon dry etching is well known.

Integration: solar cell process

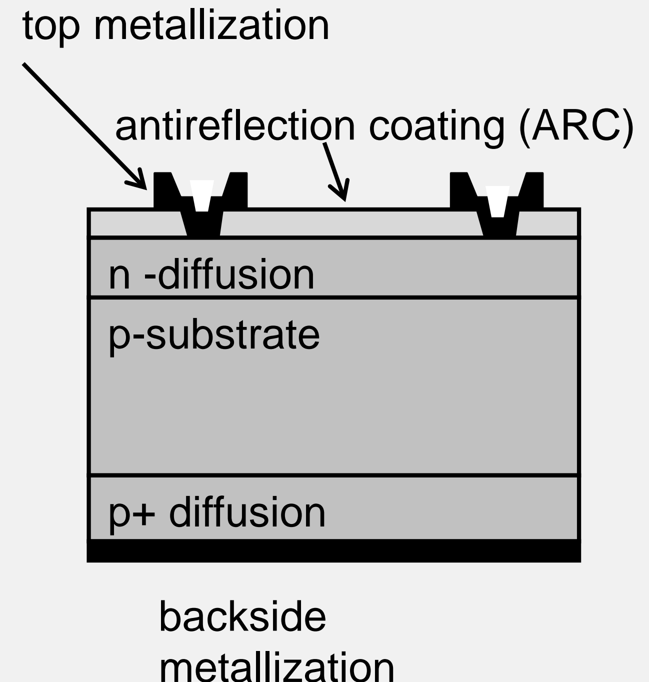


1. The contact holes in anti-reflective coating are non-critical
2. The metallization alignment to contact holes is critical

(in case of misalignment, metal does not fully cover holes, and gases, liquids, dirt can penetrate into silicon)

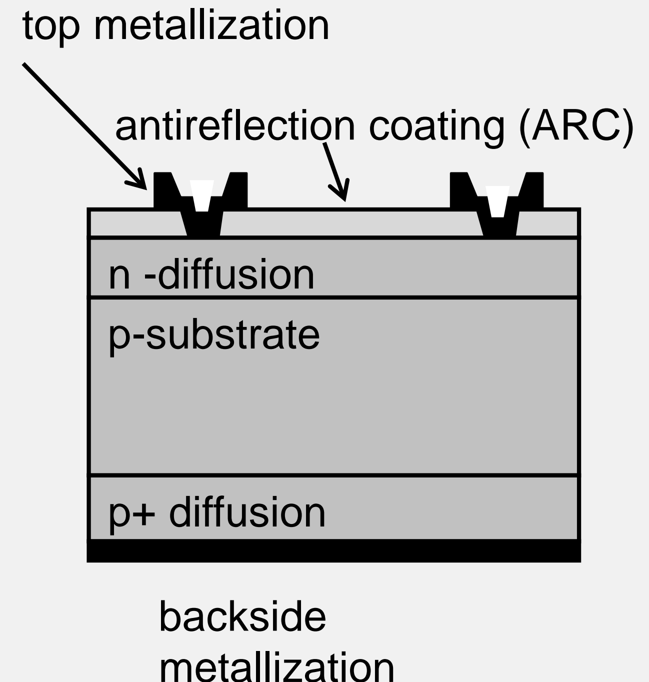
Front end processing, i.e. before metallization

- active wafer selection (thin p-type)
- wafer cleaning
- thermal oxidation
- photoresist spinning on front
- backside oxide etching
- resist stripping
- wafer cleaning
- p+ back diffusion (boron 10^{19} cm^{-3})
- front side oxide etching
- wafer cleaning
- n-diffusion (phosphorous 10^{17} cm^{-3})

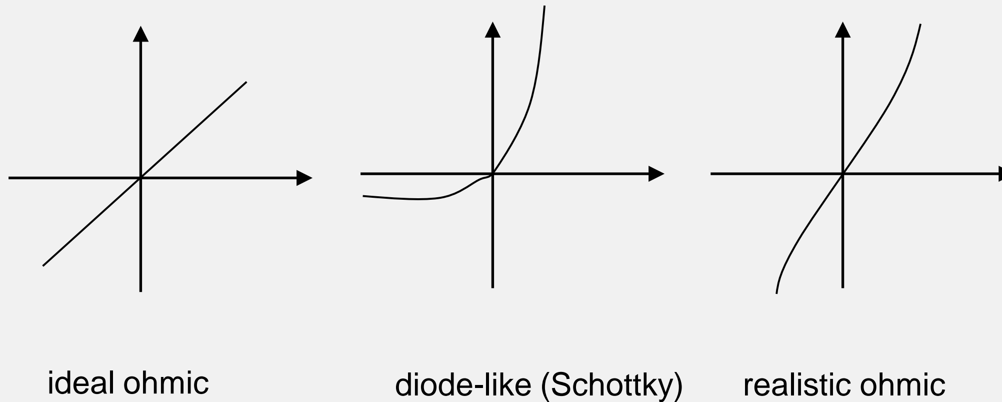


Backend processing, i.e. after first metal deposition

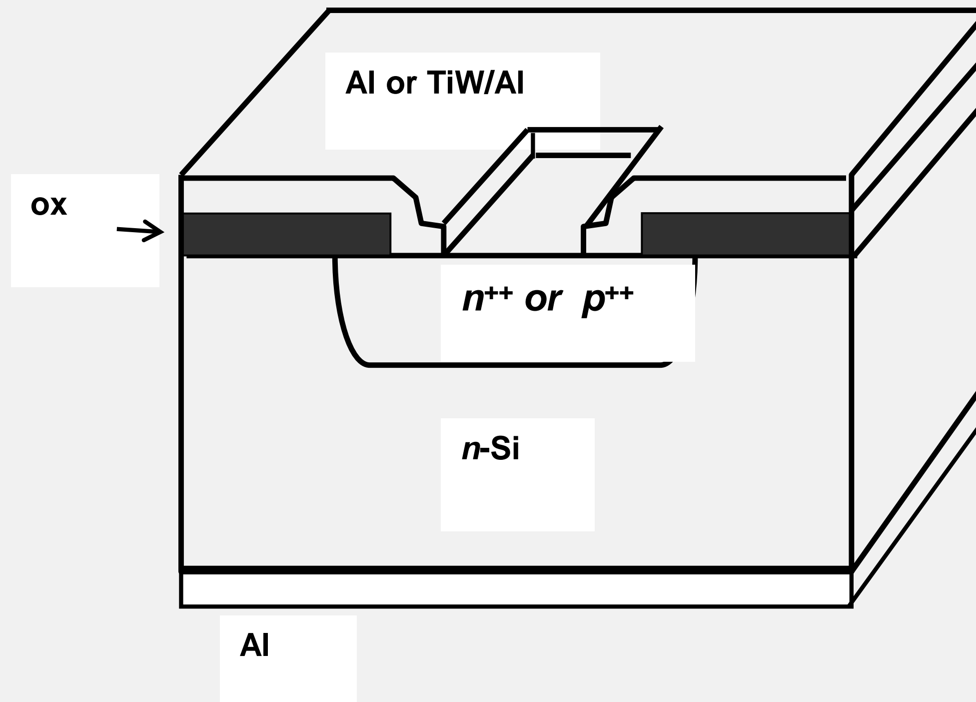
- resist spinning on front
- metal sputtering on back side
- resist stripping
- wafer cleaning (acetone + IPA)
- PECVD nitride deposition (ARC)
- lithography for contact holes
- etching of nitride
- resist stripping
- wafer cleaning
- metal deposition on front side
- lithography of front metal
- metal etching
- photoresist stripping
- contact improvement anneal



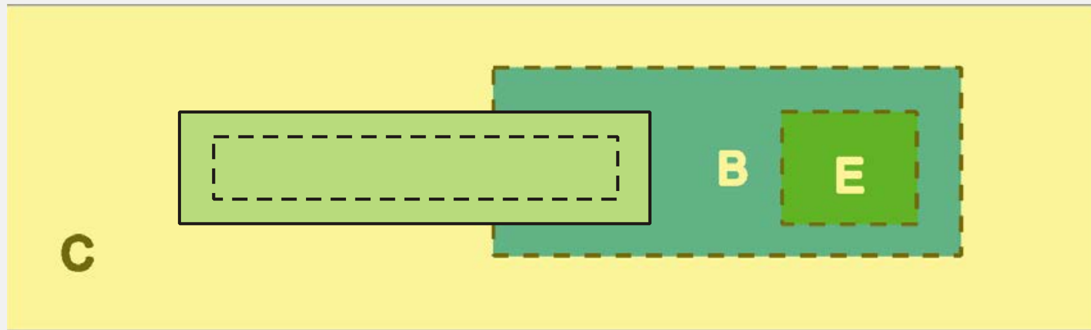
Metal-semiconductor I-V curves



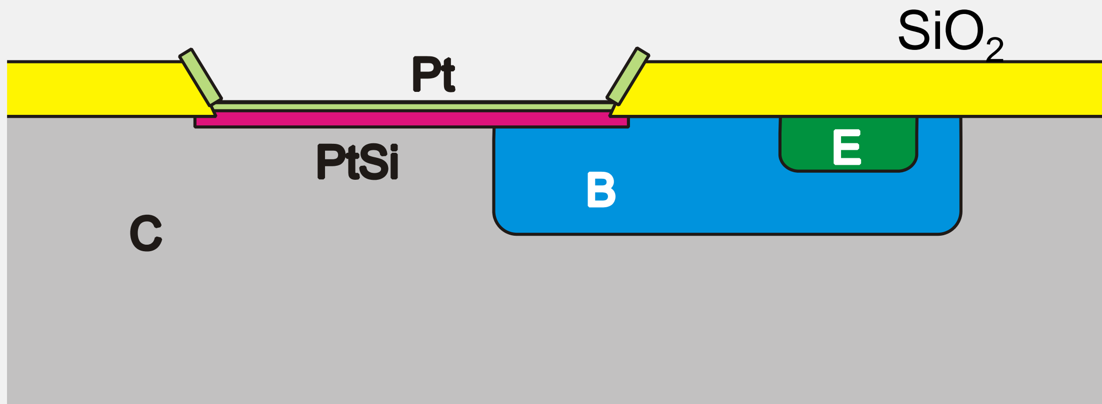
Ohmic contact



Schottky contact in bipolar transistor



PtSi/*n*-Si
Pt – 50 nm
550 °C



Metallization issues

- resistivity: ρ (thin film) > ρ (bulk)
- contact resistance to silicon (both to *n* and *p*-type)
- thermal stability: melting point; diffusion
- electromigration resistance (current density limits)
- chemical stability: cleaning
- chemical stability: oxidation, corrosion, silicidation
- deposition: phase/texture/grain size
- deposition: adhesion/stress/hillocks
- deposition: step coverage
- surface morphology and reflectivity (next deposition/lithography)
- volatility of halogenides (plasma etching)

Materials stability at high temperatures

- high temperature (>900°C; diffusion fast):

  really only Si, SiO_2, Si_3N_4, SiC
- intermediate temperature (450-900 °C):

  refractory metals not in contact with Si
- metal compatible temperature (<450 °C):

  Si/metal interface stable, glass wafers
- polymer compatible (<120 °C):

  evaporation, sputtering (lift-off resist)

Thermal budget

Time-temperature limits that the device can endure.

High temperature causes:

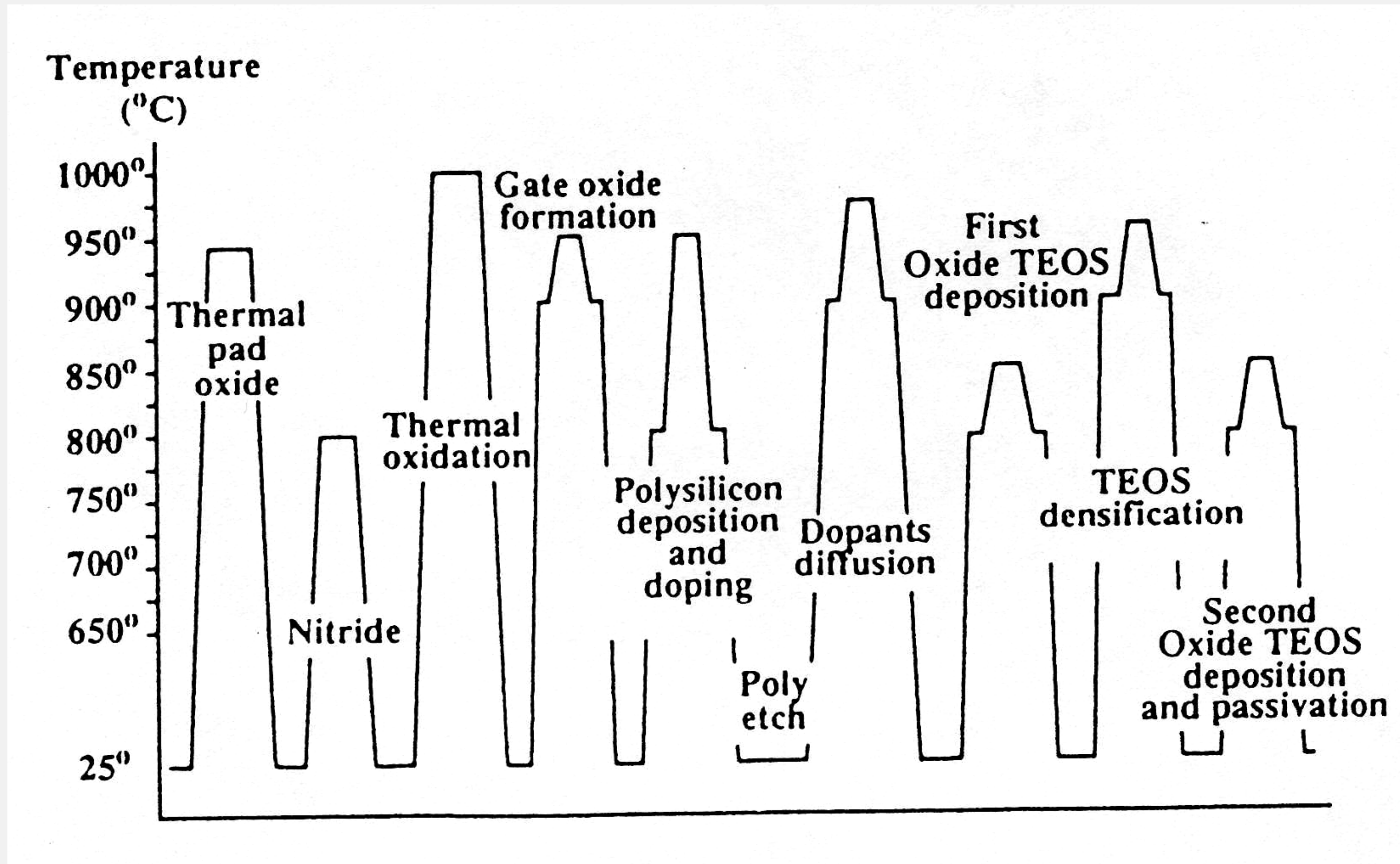
-diffusion (in all atmospheres)
-oxidation (in oxidative atmosphere)
-damage recovery, grain growth

Some of these are wanted effects, some are problems:

-implantation damage removed
-dopants driven deeper
-silicon oxidation competes with diffusion

Front end process

CMOS thermal budget



Annealing effects: physical

- grain growth (in polycrystalline materials)
- crystallization (in amorphous materials)
- diffusion of dopants (e.g. boron in silicon)
- melting (e.g. aluminum melting point 653°C, very low)
- thermal expansion and thermal stresses
- desorption of adsorbed specie

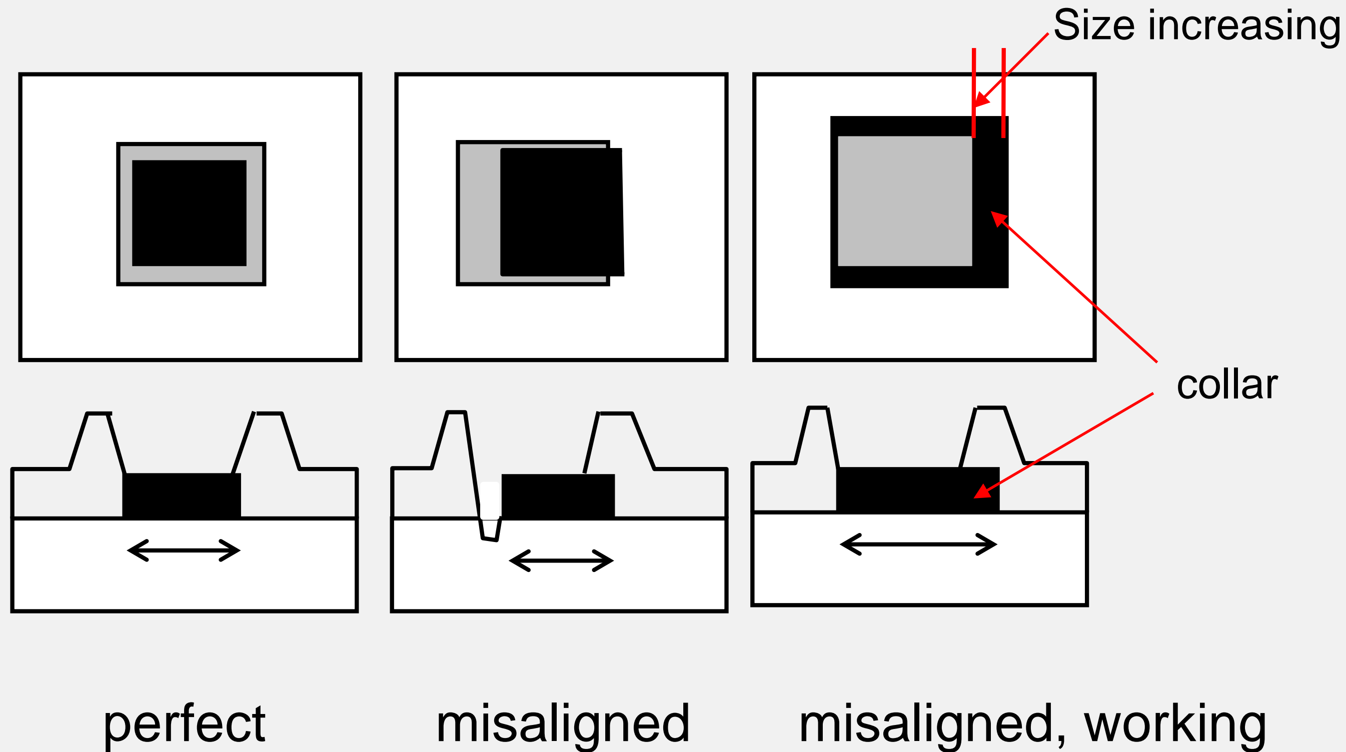
Annealing effects: chemical

- oxidation of surface: $Ti + O_2 \rightarrow TiO_2$
- reactions between thin films ($Al_{12}W$)
- reactions between substrate and thin film ($TiSi_2$)
- dissolution (e.g. silicon dissolves into aluminum)
- corrosion (Cl residues: $AlCl_3$)

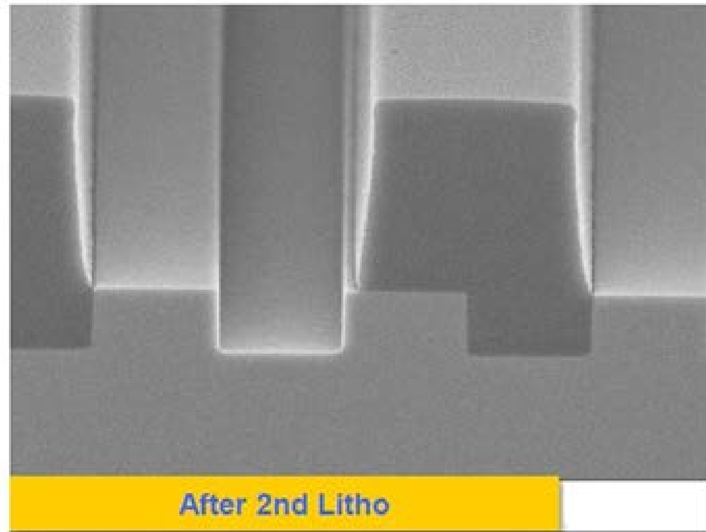
Patterns

- Lithography tools define: wavelength, mask and wafer size, chip size
- Wavelength defines PR, mask plate and resolution
- PR polarity is connected with PR type
- Mix-and-match lithography is cheap alternative
- Undercutting and mask biasing eat Si and resolution
- Device chips, test chips and alignment marks

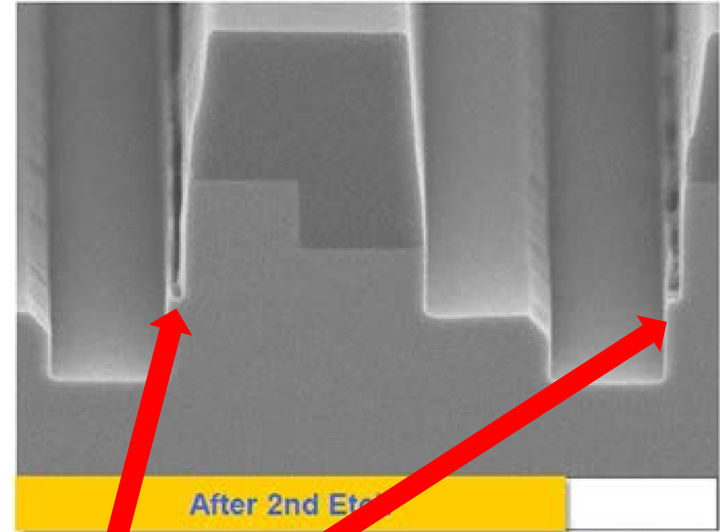
Contact-hole alignment I



Alignment error + etching



Si Etch



- Step width: 1μm
- Step height 0.5 μm
- Overlay error <100nm

This is not what you want: depends too much on alignment success.

Design rules I

a) Correct mask size and perfect alignment

b) Correct size but misaligned

c) Correct alignment but mask size error

Design rules II

Top electrode is made smaller than bottom electrode, to make sure that it lands on capacitor dielectric on planar area.

Capacitor area

Au-coil

CVD ox-3

CVD ox-1

nitride

fused silica

capacitor

Mo resistor

SiCr resistor

Design rules III

Minimum linewidth rule
Minimum spacing rule

} Within one layer

Initial assumption: minimum LW = minimum space

Overlap rules for structures on different layers

Breaking design rules ruins your process
(=you are expecting too much from the process)

Conclusion

- Microfabrication process development is very long engineering process
- It demonstrates trade off between functionality and packing density in microfabriction
- Process integration is practical realization of conceptual design